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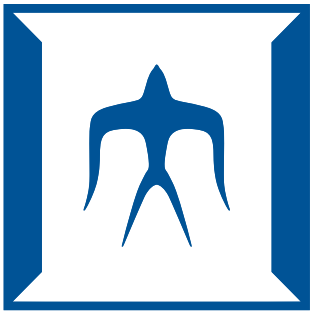

Low-Power and Small-Area RF Transceiver Front-End with Direct Antenna Interface

by

Zheng Sun

A Ph. D. dissertation submitted in partial satisfaction of the requirements for the degree of

Doctor of Philosophy

in

Department of Physical Electronics

in the

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of

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Supervised by

Prof. Kenichi Okada

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To my family,

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Abstract

This thesis presents low-power and small-area Bluetooth Low-Energy transceiver for short-range internet-of-things applications. To realize small size and long life-time modules, architecture considerations and key building blocks are discussed. An integrated radio-frequency input-output embedded with transmitter/receiver switch function and on-chip impedance matching is proposed. The proposed radio-frequency input-output is designed with minimized noise factor penalty for high-sensitivity receiver operation and harmonic suppression function for satisfying the out-of-band spurious emission requirements. To lower the power consumption and mitigate the supply variation with small on-chip area, a transformer-based low-power voltage-controlled oscillator with supply pushing reduction is presented and discussed in this thesis.

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Chapter 1

Introduction

1.1 Internet-of-Things and its Available Wireless Standards

The earliest concept of network-connected smart devices originated in 1982 with a drink vending machine that reports its inventory and temperature with connected internet [1]. After several decades of development and research, the application of the Internet of Things (IoT) has been extremely expanded and innovated. Now, the IoT covers huge industries and lots of application scenarios in life, which is much different from the first originated concept with much more content. Fig. 1.1 shows several important and main application cases. Autonomous driving, also well known as a self-driving car, seems unrealizable decades ago. However, it already gradually developed and commercialized. That should thank the development of various engineering technologies, such as computer science, sensor, communication, and the Internet. At present, there are mainly two ways to realize autonomous driving. One is mainly based on the self-intelligence of the vehicle, which requires various sensors embedded and through the local brain of the car. However, these kinds of technology consume high costs and are limited by the surrounding environment. Handling the various information in a complex environment is difficult and unreliable. Another way is the Internet-based technology, in which the vehicles and monitoring equipment can be connected over the air, *e.g.,* traffic light, even the people passing by, as the Fig. 1.1 shows. With the information chain between the people, vehicles, sensor and monitor and Internet, hardware requirement is greatly reduced and robust in the complex environment. As lifestyles change, many more smart devices are applied with our human body, *e.g.,* smartwatch with a heartbeat monitor, which can collect the data of our bodies and share with family members or even medical institutions in case of emergence. Not just the smartphones and the computers, every controllable item we can find in our

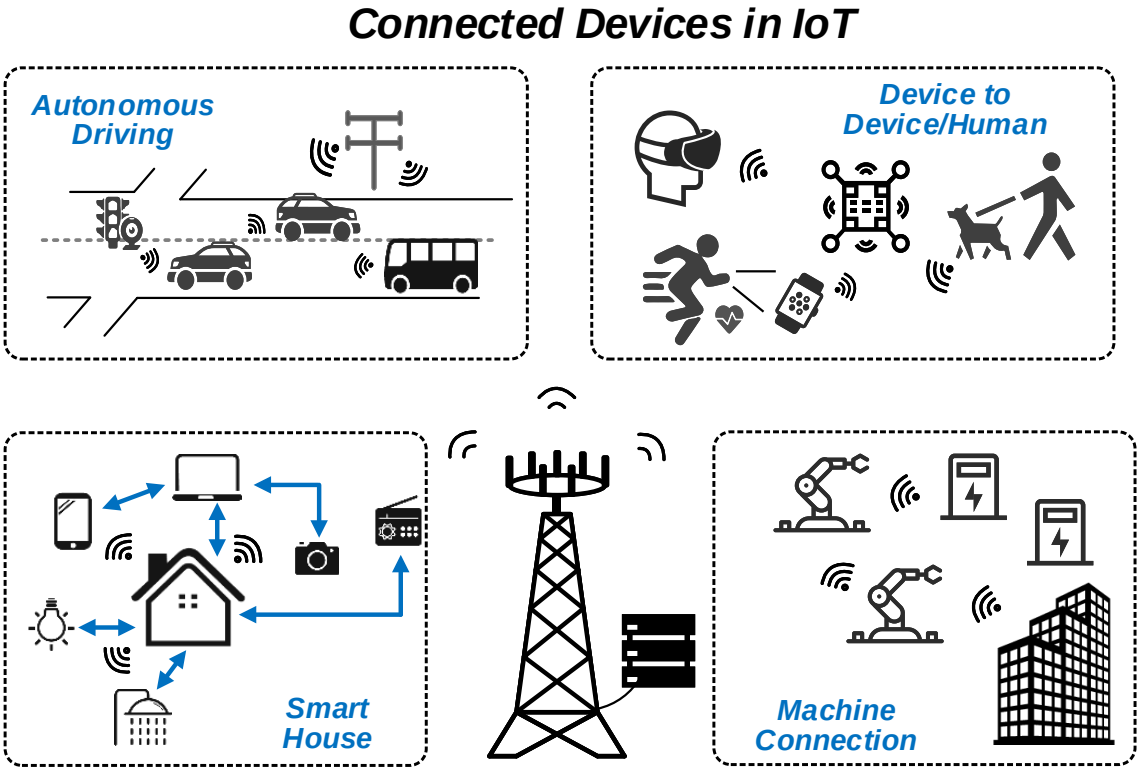


Figure 1.1: The concept of the Internet of Things.

house can be connected. Those devices can communicate, send useful information and take your words as commands. What we called the smart house or home automation is also based on the IoT. Take the light as an example. With an Internet-connected light bulb, the turn-on or turn-off operation can be remote and easily realized through the voice, evading the manual operation greatly. With the embedded sensor in the human body, the light control can be much more effective and energy harvested with monitoring our position in the house. Since the sensor also can collect the information of our bodies and even the mental, the light condition can be controlled to make people feel most comfortable. Body temperature also can be monitored and direct control the air conditioner and the direction of its fan. Through connection, those conventional devices in the house controlled with a smart brain with artificial intelligence help life in such a house become more comfortable.

Finally, the infrastructures of the city or big factory also can form a large wireless network. With connected through the Internet, the information can be uploaded, and each device can be monitored. That is a little bit like the first smart device introduced in the beginning. However, the content is much more complicated and different. Also, the amount of data are greatly increased because of the massive and various equipment. For exam-

ple, the communication between the machines and the power devices can be useful in the management of the factory. The labor cost can be heavily reduced with the automatic power control, and also, the machine status can be monitored using a remote terminal.

All those mentioned applications and networks are greatly benefiting from the popularity of wireless Internet that enabled by a various cellular network. As already popularized WiFi network, the small network with an available wired network interface will be easier to connect to a gateway device by using devices like WiFi routers. Moreover, the WiFi router will be connected to a large cellular network connected by fiber optic or 5G network. Finally, all the devices in the small networks can form a massive device's network. With the help of the computing sources such as cloud servers or smart terminals, a large amount of data can be further processed and feedback to the devices to make life better. An era full of smart devices is approaching, which can give anyone a better life if the IoT and the required wireless techniques can be further developed and exploited.

1.1.1 Medium-Range and Long-Range Wireless Standard

LTE-Advanced: Conventional LTE is known as 3.9G of telecommunications developed by the 3GPP (3rd Generation Partnership Project). In telecommunications, this one was also promoted with the name "4G LTE". The initial LTE does not meet the technical criteria of a 4G wireless service, as specified by the 3GPP (Release 8 and 9 document series for LTE Advanced). Since 2011, the LTE-Advanced standard has been commercialized. This standard uses several frequency bands (from around 1 GHz to 6 GHz) with associated different bandwidth.

5G: As well know, 5G is the fifth generation technology standard for cellular networks. The low-band of 5G (FR1) uses a similar band as the LTE (< 6 GHz). While the new 3GPP specification series 38 provide more technical details. In the newly released 5G NR standard, high-band 5G (FR2) uses frequencies from 25 GHz to 39 GHz, almost achieve the millimeter-wave band. However, higher frequencies may be used in the future. This standard targets much faster wireless communication, such as gigabit per second. Not like the millimeter wave standard, which has a much-limited communication distance, the 5G NR can be applied in medium-range telecommunications, and has been firstly commercialized in 2019.

NB-IoT: It is also standardized by the 3GPP (release 13). This standard uses the LTE

technology subset but with much narrow bandwidth (200 kHz). This standard mainly focuses on the coverage range and the connection density.

Long-range Communication: There are several standards for long-distances communications, such as LPWAN. These standards typically use ultra-narrow bandwidth and ultra-low data rate, *e.g.,* 0.3 kbit/s.

1.1.2 Short-Range Wireless Standard

WiFi : It has family standards based on the IEEE 802.11, and this standard has been developed for more than twenty years. It operates at the ISM band in the sub-6 GHz, which including the 2.4 GHz, 3.6 GHz, and 4.9/5.0 GHz bands. A high date rate can be realized from several Mbps to several Gbps. This standard is straightforward to be implemented with a wired network interface within a few tens of meters. For the newly released WiFi 6 standard, which is based on IEEE 802.11ax, a higher-order modulation method has been implemented, and a higher data-rate can be achieved.

ZigBee: It is a short-range wireless standard based on the IEEE 802.15.4. This standard operates in the 2.4 GHz ISM-band with 250 kbps data rate suitable for the intermittent data transmission from the sensors and duty-cycled devices. The maximum number of nodes in the Zigbee network is 1024. Depend on its working environment and power configuration. The communication range can be controlled from tens of meters to hundreds of meters.

Light Fidelity: A communication method utilized the light emitted by diodes (LEDs) as the information carrier. Due to the characteristics of visible light itself, this standard can be effective in confidential communication that can't get through the wall or the door. Moreover, this standard is useful in the special situation without causing electromagnetic interference such as hospital and the airplane.

NFC: Near-field communication is a protocol for two devices which has a short distance lower than 4 cm. This protocol is well known because of the identity cards and the contactless payment. In a current new type of mobile phone, the NFC is integrated, which can be used for mobile payment and the tramcar ticket like the PASMO.

Bluetooth Classic: As the most famous wireless standard within tens of meters, Blue-

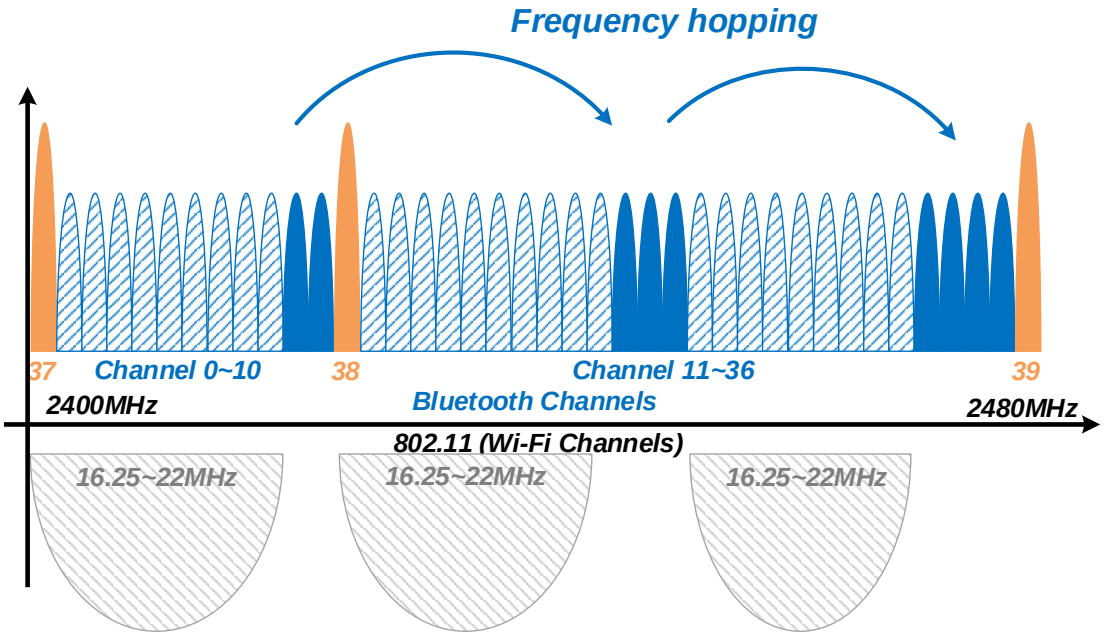


Figure 1.2: The channels of Bluetooth standard and its coexistence with Wi-Fi.

tooth has been widely used in electronic devices around us, such as the mobile phone and headphone. This standard has been proposed since 1994 and has been iterated and upgraded into several versions. This standard operates at 2.4GHz, which is located in the globally unlicensed ISM frequency band. The variable data rate and robust implementation make this standard widely used in audio streaming and file transmission.

Bluetooth Low-Energy: Different from the classic Bluetooth standard used for continuous audio streaming, Bluetooth Low-Energy (BLE) is an ultra-low-power version of Bluetooth (4.2). The main target devices are the applications that do not require continuous connection and intermittent data transmission, *e.g.,* disposable sensors, but depend on long battery life and costs.

1.2 Bluetooth Transceiver and its Applications

After decades of evolution from 1994, *Bluetooth* technology becomes one of the most popular wireless standards in short and middle-range communications using short-wavelength UHF radio waves in the ISM bands, from 2.4 GHz to 2.4835 GHz. The RF channels are specified to 1 MHz, while the band each channel is 2 MHz. Together with WiFi technology, it is widely adopted in almost all kinds of wireless communications. As shown in

Fig. 1.2 , three advertising channels (channel 37, 38, 39) for the device discovery, connection establishment, and broadcast transmissions. To robust co-exist with the WiFi signal working on the same ISM band, which has a much wider channel bandwidth. A mechanism called adaptive frequency hopping is adopted. This mechanism is used by the link layer, and the link-layer will remap a given packet from a known bad channel to a known channel without interference, *e.g.,* a WiFi signal. Through that, interference from other devices is reduced. This technology really makes the Bluetooth transceivers robust work in the complex environment where the microwave oven, other Bluetooth devices, and WiFi devices co-exist. Because of its robustness and easy implementation, the Bluetooth transceivers have become much popular with various applications.

For now, the most famous application scenario is the smartphone integration and replacing the conventional wired solutions, such as earphones and keyboards *etc.*. For the Bluetooth standard beginning, the Institute of Electrical and Electronics Engineer (IEEE) standardized this standard as IEEE 802.15.1 at the beginning of this century. However, it is no longer maintained by IEEE. Now a special interest group (SIG) [2] oversees the development of these standards as well as protects the trademarks. It was established by IBM, Intel, Nokia, and Toshiba, and later joined many other companies. Now, the Bluetooth SIG is a global community of over 36,000 companies serving to unify, harmonize and drive innovation in this Bluetooth standard. In order to meet the requirement of the market and uniform standards, the manufacturer or the developer must satisfy Bluetooth SIG standards before releasing to the market.

Also, because of the Bluetooth transceiver work in the ISM band, which is a globally unlicensed frequency band, the transceiver implementation also must satisfy the regulations required by the local government, such as the Federal Communications Commission (FCC) in the United States. For example, the transceiver operating with the frequency band from 2400–2483.5 MHz must satisfy the FCC 15.247. Otherwise, any devices with the substandard Bluetooth transceiver cannot be sold in the United States.

The core specification has been updated from version 1.0 (1998) to version 5.2 (December 2019). In the standard V4.0, the low-energy controller part is added, which has many differences from the previous basic rate (BR) or enhanced data rate (EDR) controller. The conventional Bluetooth addresses the point-to-point communication, such as the audio streaming for the laptop to the audio speaker shown in Fig. 1.3. The high sound quality requires the higher data rate of the Bluetooth transceiver. Typically, the Bluetooth basic data rate mode with 1 Mbps and enhanced data rate 2/3 Mbps mode are sufficient for these applications.

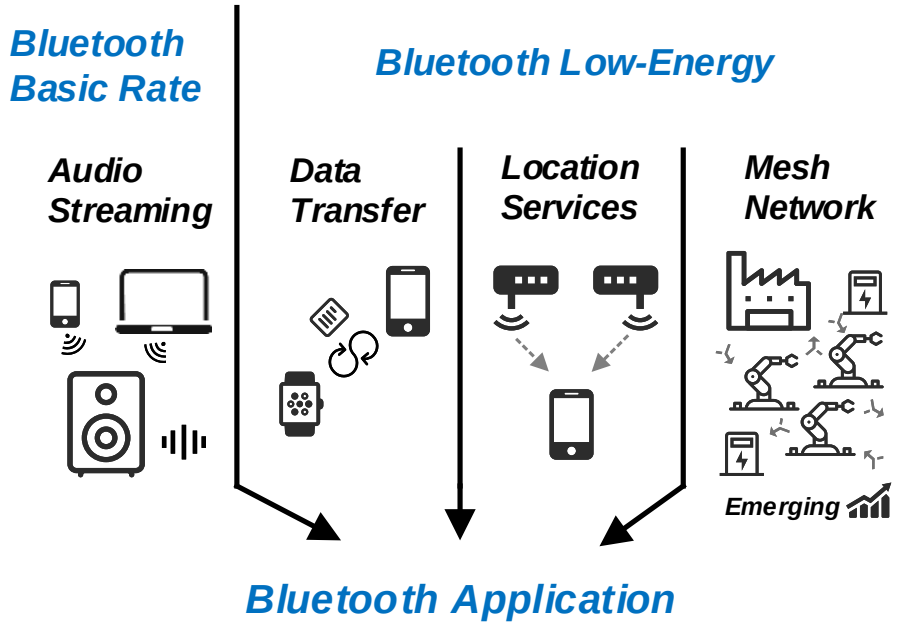


Figure 1.3: The applications of Bluetooth and its classification.

There are several important differences of the Bluetooth Low-Energy listed below.

Lower Power: The low duty cycle such as 0.5 s to 10 s intervals. The scenarios for which the period of interaction is large, and there is a very relaxed latency. The temperature and humidity monitoring are the typical scenarios. The leakage power of the transceiver is also design low. Thus, the average power consumption is quite small, which can be clearly expressed by the following equation.

$$DC_{\mathrm{AVG}} = \frac{DC_{\mathrm{operation}} \times T_{\mathrm{DC}} + DC_{\mathrm{leakage}} \times (T - T_{\mathrm{DC}})}{T} \tag{1.1}$$

From this equation, different optimizations for low power consumption to achieve a long lifetime can be taken into different scenarios [3]. For example, a continuous high frequency is scenarios for which the operation cycle dominates, *e.g.,* heart rate monitors that communicate measurements several times in seconds to trackers. More accurate counting requires more operation cycles in seconds, which is a trade-off with the operation power. Thus, the DC power for the operation should be optimized. Another periodic low-frequency scenarios are the applications that have a long standby time, *e.g.,* temperature monitoring, which has a gradually transformation. In this kind of application, the operation cycle can be very small such as one cycle (<10 ms) in tens of seconds. The leakage power of the transceiver will dominate the total average power consumption.

Table 1.1: DETAIL DIFFERENCES BETWEEN BLUETOOTH BR/EDR AND LOW-ENERGY

Characteristic	Bluetooth BR/EDR	Bluetooth Low-Energy*
Discovery	Inquiry	Advertising
RF Channels	79 Channels	40 Channels
Number of Piconet Slaves	7(active)	Unlimited
Modulation Method	GFSK/DQPSK, 8QPSK	GFSK
Max Data Rate	1/2,3Mbps	1Mbps
Typical Range	>10 meters	>10 meters
Output Power	100 mW**	100 mW**

* Core version 5.2
** Power Class I

Faster Connection: The low-power consumption is a benefit from its fast connection operation. For a classic Bluetooth transceiver, a link-level connection can take up to 100 ms, which means more power is wasted in the long connection progress. For a BLE transceiver, the devices can connect and send and acknowledge data in 3 ms. That requires the BLE transceiver has a much faster mode switch function, which can send and acknowledge data individually.

Table 1.1 summarized the detailed differences between Bluetooth BR/EDR and Low-Energy. While the Bluetooth BR and EDR address the point to point communication. The Bluetooth expanded into broadcast communications to enable indoor positioning and location services, as shown in Fig. 1.3.

BLE devices support several roles in these applications,

Data transfer Application: The smartwatch performs a master device that scans for advertisers. If there is a new message comes, the smartphone will operate as the advertiser. The connection between the phone and watch can be initiated since the BLE is designed with a faster connection. This application can be effective in the broadcast in crowded places.

Locations Services: Several position fixed beacons will be placed surround. This function relies on a property known as the received signal strength indicator (RSSI) to calculate how close a beacon is from the device. According to the beacon number, more precision can be realized.

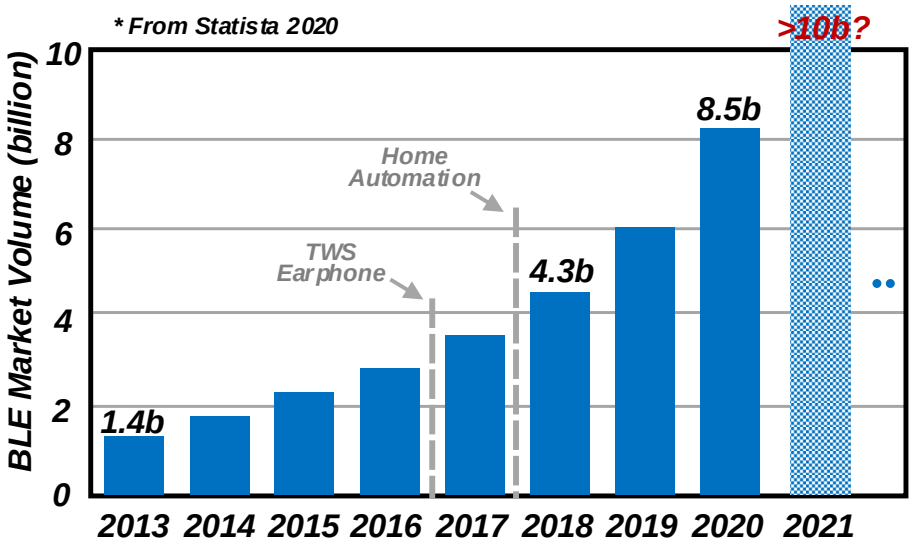


Figure 1.4: The market volume of BLE applications and its trend.

Mesh Network: Since the BLE is designed as a reliable wireless solution to establish large-scale device networks. A mesh network can be established with the BLE. This concept originated from a massive network. The topology is that one of the "node" (device) transmits its own data, and this device also serves as the relay for the nearby "node". All the nodes can be practices to form the most efficient data transmission path. Even, some failures happen in some "nodes", the other path through the working "node" will still continue to deliver the information. That ensures the connectivity is always working and reduce the cost from the failure nodes.

The variety of the roles and features present very good support for different application scenarios with low distance and moderate/slow date rate. It is the main reason that Bluetooth standard with additional BLE becomes one of the most popular wireless technology for IoT applications. From the data website Statista 2020, as shown in Fig. 1.4, the BLE market volume has been increased from 1.6 billion in 2013 to nearly six times until now. And it can be predicted from the data, the marker volume of the BLE will still increase and break the 10 billion record, which no other standards can reach. The emerging new applications such as the True Wireless Stereo (TWS) earphone and home automation boost the accelerated the market volume growth of BLE.

1.3 Challenges for RF Front-End Design with Direct Antenna Interface

1.3.1 General Challenges for BLE TRXs

The general challenges for BLE transceivers are considered for both industry and academic aspects.

Low Cost: The cost is the main important point for the low-end Bluetooth manufacturers to enter the market. Low-price means more market share while increasing shipments. The increased shipments help further reduce costs. Furthermore, this positive feedback will allow a company to beat others to occupy all low-end market shares.

Low-Power Consumption: The power consumption for the BLE application is also important, which will be mainly used in wearable devices and wireless sensors. Those devices do not need to keep running at all the time, and they are only wakened up to perform data transmission for a short time. However, due to the size limitation according to the application scenario, a long lifetime is desired with a small battery capacity. That requires the BLE transceiver works with low-power consumption and low stand along with power.

Small Module Size: As mentioned before, the main applications of the BLE transceiver include wearable devices and sensors. In the real application, the module of the BLE transceiver includes the PCB, and the off-chip components (*e.g.,* trace antenna) takes a much larger area but with lower cost. Some kinds of BLE modules integrate internal antenna, which reduces off-chip area but increases the module cost.

Signal Accuracy and Stability: For the high-end market, a stable and excellent performance will be more important. Such for the indoor positioning, and accuracy RSSI is required. That means the TX power should be precisely controlled, and RX demodulation should be very accurate overall for possible environmental changes.

Low latency and fast link: A shorter link establishment also means lower power consumption with reduced operation time. Meanwhile, the interference will cause the performance degradation of the BLE transceiver, which will heavy the latency of BLE communications. This kind of performance is also a mark for high-end BLE products.

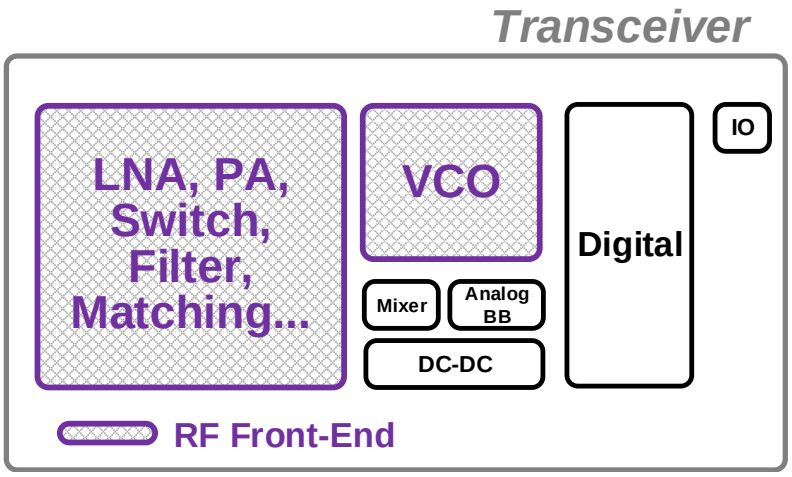


Figure 1.5: The general structure for wireless transceivers.

1.3.2 Academic Challenges

In this thesis, only academic challenges listed below are mainly considered due to personal ability and time constraints. The other aspects without here can be considered as future upgrades or work in the industry.

Lower Cost: As an industry product, the BLE modules must have stable performances, and typically, the conventional structure of circuits will be applied to reduce the risks while trading with the on/off-chip area. However, in academia, the new circuit structure can be tried without considering commercialization. Meanwhile, the off-chip components are typically implemented to reduce the difficulty of full integration and avoid performance degradation. In here, we mainly consider the feasibility of reducing the off-chip components and try to realize the nearly same performance with reduced off-chip component numbers and smaller on-chip area.

Lower Power Consumption: The low-power techniques are seldom reported by the industry company. It's not to say that they don't have low-power technologies, but that they often add a lot of power in order to obtain stable performance. In academic consideration, the feasibility of the lower power consumption method can be certified with new circuit techniques.

1.3.3 Fundamental Issues

For IoT applications, large-scale popularization will inevitably require cost reduction of wireless transceiver modules, including the IC cost and PCB cost. As we know, there are mainly three types of IC cost, which includes the die cost (> 50%), testing cost, and the packaging cost. The die cost is determined by the wafer cost and the number of dies per wafer. That means the small chip area will reduce the average IC cost. This saving will be more evident for more advanced processes. The implementation of off-chip components can realize very outstanding performances. However, it is inevitably to increase the PCB cost and finally increases the module cost.

Fig. 1.5 shows the general structure of wireless transceivers. As we know, the passive components cannot be shrunk with the process scaling. Moreover, these components occupy most of the on-chip area because of the large inductors are required in these circuits, such as our LC-type oscillator. Meanwhile, for the oscillator, specified phase noise must be satisfied to achieve the target transceiver performances (the detailed PN performance required will be discussed in the next sub-section). Typically, for the low-power IoT application, the phase noise performance is not critical. Meanwhile, the on-chip area becomes much important because of the cost.

Another one that takes up much on-chip area is the RF input and output circuits. These circuits, such as LNA, PA, and switches, can be designed with off-chip components. However, that will heavily increase the off-chip costs and area. Typically, for the LNA, at least three inductors are required (for the cascode LNA), and at least two inductors are required for the PA (class-D PA with LC-notch filter). The total number of inductors is almost unchanged in the conventional design. Meanwhile, to share a single antenna, the antenna switch must be integrated by using on/off-chip switches. In this thesis, we mainly focus on how to realize a low-power design while reducing the on-chip area by reusing the passive components (not limited to inductors) and mitigating the usage of off-chip components. We want to realize a fully integrated BLE transceiver with minimized the on-chip area and power consumption while meeting the FCC requirements.

Thus, to reduce the cost of the wireless transceiver as much as possible so that it can be popularized in life, this thesis focuses on the small-area front-end design, including the RF input/output circuit and frequency synthesis circuits.

1.3.4 Specification Consideration

Fig. 1.6 shows an example of a BLE transient power breakdown from a commercial SoC (CC-series, Texas Instruments). The transceiver will be waked up by the triggers from the wake-up receiver embedded. And then pre-process will start. Before the receiver works,

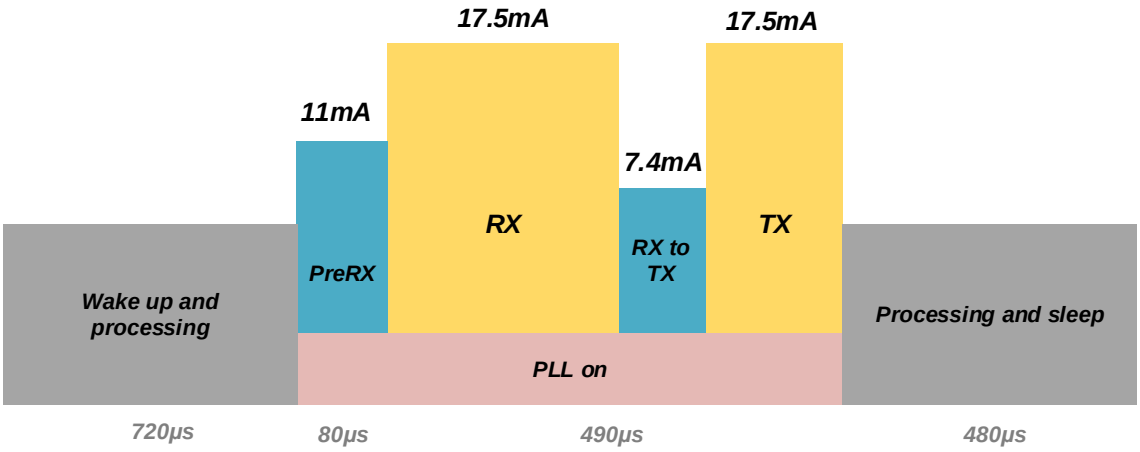


Figure 1.6: Power breakdown of a Texas Instruments CC-series BLE device in a single connection event.

there is a pre-RX procedure to configure the transceiver into the receiver mode. After the desired signal is received, the transceiver will be re-configured, and then the TX will start to work, which sends the data out as the response of the received signal. From Fig. 1.6, the power consumption of the transceiver is clearly shown. As explained in Chapter 1.2, for the a continuous high-frequency scenarios, the power of the operation cycle dominates the average power consumption and thus the lifetime. For a conventional 2.4 GHz transceiver, there are a lot of low-power techniques to lower the power consumption. However, as a globally unified standard, the Bluetooth Low-energy transceiver must satisfy the core specification. Only considering the specs and the power budget at the same time, power reduction is effective. Firstly, the analysis of the difficulties of BLE specification and transceiver implementation should be carried.

Transmitter Characteristics based on core specification V5.2 [4] are summarized in Table 1.2. Total 40 channels are assigned from 2.4 GHz to 2.8 GHz with 2 MHz channel spacing. However, the output power is enhanced and multiple classes are selectable. Also the data rate is not fixed to the 1 Mbps and a 2 Mbps is also as one of the options in V5.2. The 1 Mbps, as the must-have option, has the signal energy concentrates from -500 kHz to +500 kHz. For each channel, there are 500 KHz exists on the left and right side of the signal, which relax the adjacent channel interference performance for the RX. For the 1 Mbps option, because of the larger signal bandwidth (2 MHz), the channel bandwidth is also increased to 4 MHz, which includes two 1 MHz blank existing on the left and right side. The frequency deviation, as shown in Fig. 1.7, is also specified to different data rate options. What should be noticed here is the minimum frequency deviation test method, which is also specified in the specification. With a data pattern 00001111, the F_{min} must

Table 1.2: TRANSMITTER CHARACTERISTICS BASED ON CORE SPECIFICATION V5.2

Parameters		Value
Channels		f=2402+k*2 MHz, (k=0, ... ,39)
Output Power		Power Class 1:10dBm∼+20dBm Power Class 1.5: -20dBm∼+10dBm Power Class 2:-20dBm∼+4dBm Power Class 3: 0dBm∼-20dBm
Modulation Scheme		GFSK (0.5± 5% modulation index)
Frequency Deviation F_{min} = min { $\|F_{min+}\|$, F_{min-} }		1 Mbps: 250 KHz (F_{min}>185 KHz) 2 Mbps: 500 KHz (F_{min}>370 KHz)
Harmonic Emission	2nd harmonic	-41.2* dBm
	3rd harmonic	-41.2* dBm
In-band Spurious Emission	1 Mbps	2 MHz: -20 dBm
		≥ 3 MHz: -30 dBm
	2 Mbps	4,5 MHz: -20 dBm
		≥ 6 MHz: -30 dBm
Frequency Drift	Package	± 50 kHz (Maximum drift)
	Drift Rate	400 Hz/μS

* According to FCC 15.249.

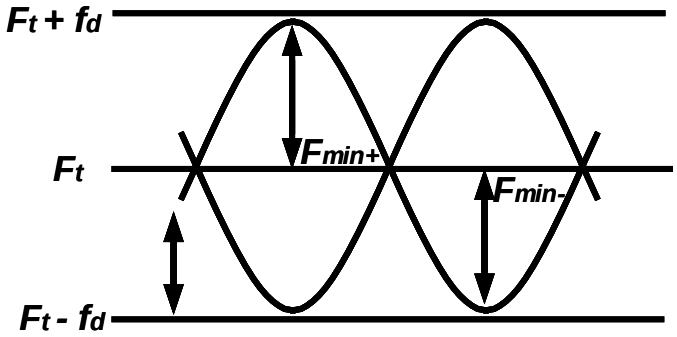


Figure 1.7: The TX frequency deviation of BLE Transmitter.

have an average value between 225 kHz to 275 kHz. With a data pattern 01010101, the F_{min} must be large than 185 kHz with the average value large than 0.8 times the average value of pattern 00001111.

The TX in-band spurious emission is generated from the non-linearity of the TX chain or the phase noise or spurious of the frequency generators (PLLs). What should be noticed that the in-band spurious emission is specified in absolute value (dBm), which is measured on a 1 MHz RF frequency range. That means with a high noise level frequency generator can't satisfy this requirement due to its noise skirt. Also, this requirement has a linear relationship with the output power. For example, for a 0 dBm output power case, the PN noise requirement of the PLL is around -100 dBc/Hz at 1 MHz offset to satisfy the in-band spurious emission. However, this noise performance must be improved to 20 dB higher (-120 dBc/Hz) if the output power is increased to 20 dBm. For a -100 dBc/Hz at 1 MHz frequency offset, a ring oscillator (RO) with around -86 dBc/Hz (with 5 MHz PLL bandwidth) can realize this performance. However, the phase noise of RO can't satisfied the high output power case which is difficult to achieve lower than -100 dBc/Hz at 1 MHz frequency offset. Also, the fractional spur of the PLL should be considered, which falls in the close-in frequency band. That makes the phase noise performance of PLL much tighter and safety margin should be left for a robust application (< -125 dBc/Hz at 1 MHz for 20 dBm output case).

TX generates electromagnetic (EM) radiation at unintentional frequencies, and the strong harmonic spurious emissions result in polluting of the out-of-band spectrum potentially, which desenses the RXs operating at the same harmonic frequency (e.g., HD2 of the 2.4 GHz TX locates band n79 for 5G NR). Actually, the harmonic emission is not directly specified by the core specification. The only requirement is that the equipment manufacturer is responsible for the ISM out-of-band spurious emissions requirements in the intended countries of sale, such as North American or Asia market. Typically, the FCC 15.249, which specified for the transceiver which utilizes the ISM band should be satis-

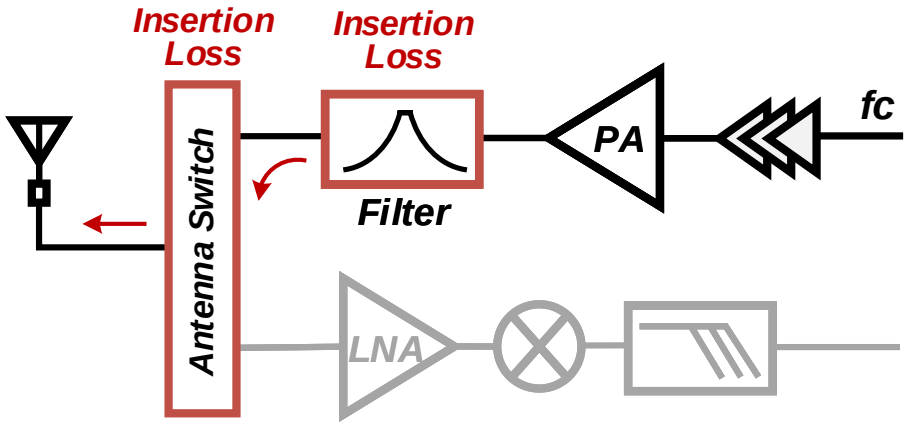


Figure 1.8: The simplified transmitter model.

fied. According to the authors' knowledge, the requirement for the ISM bands transceiver is also similar as the ETSI standard (ETSI EN 300 328). The specified field strength of harmonics E_0 is in micro-volts/meter (500 μV/m specified at a distance of 3 meters) in the FCC standard, which can be converted into an equivalent -41.2 dBm as a conducted power (equivalent, sometimes "effective", isotropically radiated power, EIRP) using the following equation.

$$EIRP(dBm) = E_0 + 20log_{10}\mathrm{D} - 108.4 \tag{1.2}$$

The corresponding electric field strength E_0 specified in FCC 15.249 is 500 μV/m, which equals 53.98 $dB\mu$V. This field strength limit is specified at a distance D equals to 3 meters. The detailed spurious emission is shown in Fig. 1.9. Because of the out-of-band spurious emission is also specified in dBm, which means the fundamental signal to harmonic distortion (HD) ratio has to be also increased. For example, in the 0 dBm output case, the second harmonic distortion (HD2) ratio is -41.2 dBc. However, this value should be increased to -51.2 dBc in the case of +10 dBm output power. That increases the difficulty of the on-chip integration due to the insufficient quality factor of the on-chip filters, which introduces large insertion loss, as shown in Fig. 1.8. Also, we should notice that power loss is inevitable in the filter implementation. It should be noticed that the on-chip filters take more chip area while off-chip filters take more PCB (off-chip) area. Neither way is economical and what we want to see today in pursuit of device miniaturization.

As the maximum frequency drift is specified in the package transmission ($\pm$ 50 kHz), this requirement, which is not strict, relaxes the local oscillator (LO) specification. Even a free-running LC-type voltage control oscillator (VCO) can satisfy this requirement due to the short length of the package in BLE (maximum size link layer data packet, 27 bytes

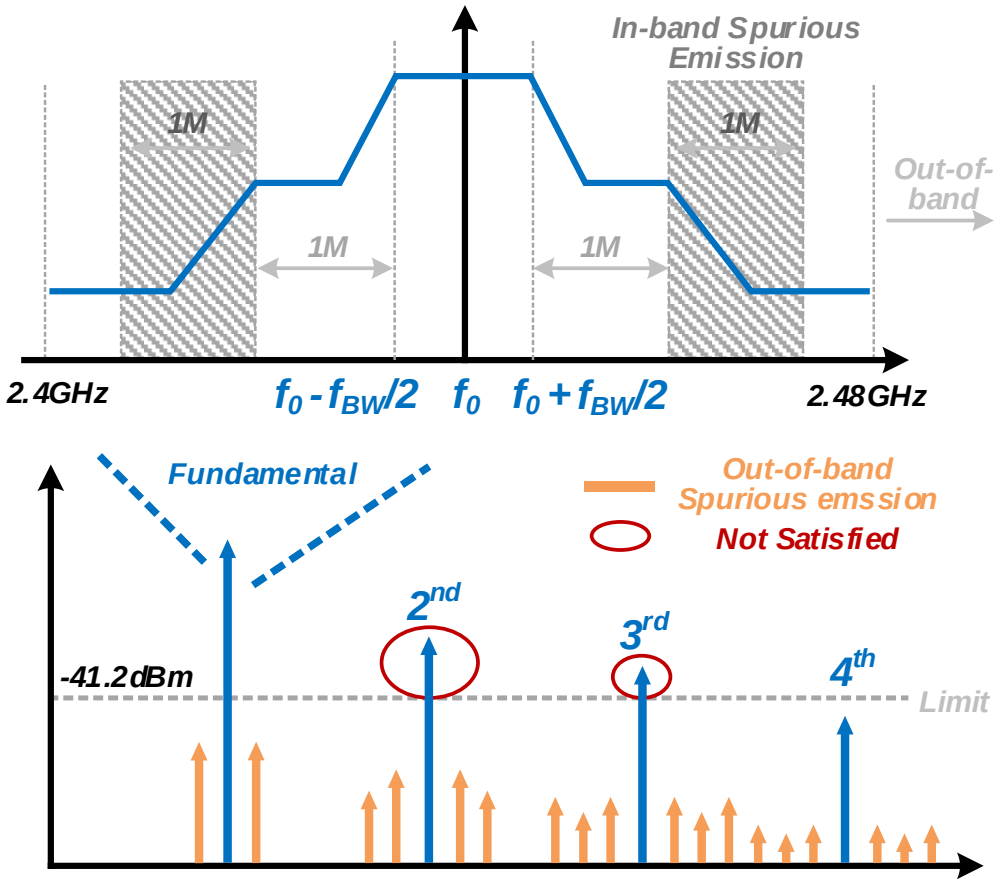


Figure 1.9: The TX spurious emissions including in-band and out-of-band cases.

Table 1.3: RECEIVER CHARACTERISTICS BASED ON CORE SPECIFICATION V5.2

Parameters		Value
Sensitivity	Spec.	-70 dBm
	Target	-90 dBm
Maximum Input Power	Spec.	-10 dBm
	Target	+10 dBm
Packet Error Rate (Bit Error Rate)		30.8% (0.1%)
Adjacent Channel Rejection	0 MHz	-21 dB
	1 MHz	-15 dB
	2 MHz	17 dB
	3 MHz	27 dB
Blocker	30∼2000 MHz	-30 dBm
	2000∼2400 MHz	-35 dBm
	2500∼3000 MHz	-35 dBm
	3000∼12.75 GHz	-30 dBm

of data in a 41-byte payload, which takes 328 μs) [5].

The summary of RX part specification are listed in the Table 1.3. The actual receiver sensitivity level is defined as the receiver input level for which specified in Table 1.3 (0.1% BER or 30.8%PER) is achieved. Firstly the received power of the BLE transceiver should be considered. To derive the received power at the input port of the receiver, the Friis transmission equation can be utilized.

$$P_{\mathrm{R}} = \frac{P_{\mathrm{T}} G_{\mathrm{T}} G_{\mathrm{R}} \lambda^2}{(4\pi D)^2} \tag{1.3}$$

P_{R}: received power at the input port of the receiver.
P_{T}: transmitted power of the output port of transmitter.
G_{T}, G_{R}: antenna gain in the direction of the another device.
D: Distance between the transmitter and the receiver.
λ: The wavelength of the transmitted signal, which equals to c/f (c: speed of light).

The terms in equation (1.3) that is independent of all the hardware, $\frac{\lambda^2}{(4\pi D)^2}$, is defined as the Free-Space Path Loss (FSPL).

$$\begin{aligned} FSPL &= (\frac{4\pi D}{\lambda})^2 \\ &= (\frac{4\pi Df}{c})^2 \\ (dB) &= 20\log_{10} D + 20\log_{10} f - 147.55 \end{aligned} \tag{1.4}$$

in which, the D is in meters and f is frequency in Hertz.

To classify the relationship between receiver power P_{R} and the FSPL, it is useful to rewrite the equation (1.3) in decibel, which has:

$$P_{\mathrm{R}}(\mathrm{dBm}) = P_{\mathrm{T}}(\mathrm{dBm}) + G_{\mathrm{T}}(\mathrm{dB}) - FSPL(\mathrm{dB}) + G_{\mathrm{R}}(\mathrm{dB}) \tag{1.5}$$

For the convenience of description, the transmitted power P_{T} is assumed to be equal to 0 dBm. While considering the traditional metal plate antennas on the market [6], the gain of the antenna is around 0 dBi. Thus, both of the antenna gains are specified in 0 dB in this estimation. In a 10 meters communication distance with a barrier-free condition, the FSPL is calculated as the 63 dB with a carrier frequency f equals 2.4 GHz. Thus, the received power P_{R} can be estimated using equation 1.5, which equals -63 dBm.

Since the FSPL will increase 6 dB with a doubled distance and the obstacle in space will increase the FSPL significantly, *e.g.,* concrete wall and wood. Thus, there are only two ways to increase communication distance. One is increasing the output power of transmitter P_{T} which consumes more TX power and in contrast to the trend of low-power. Another way is to design a receiver with high sensitivity. In the example just described, the received power at 10 meters is just -63 dBm in an ideal case. The receiver sensitivity must be less than or equal to this number to make sure the requirement of the BER can be satisfied with a -63 dBm input signal. The sensitivity of the receiver can be estimated using the following equation.

$$\begin{aligned} Sensitivity &= 10\log_{10} KT + 10\log_{10} BW + NF + SNR_{modem} \\ &= -111(\mathrm{dBm}) + NF(\mathrm{dB}) + SNR_{modem}(\mathrm{dB}) \end{aligned} \tag{1.6}$$

BW : the channel bandwidth (2 MHz).
K, T : 1) Boltzmann's constant in Joules/°K, 2) temperature in °Kelvin.
NF : the cascaded receiver noise figure in dB.
SNR_{modem} : The minimum signal to noise ratio required by the digital modem to satisfy the specified BER or PER.

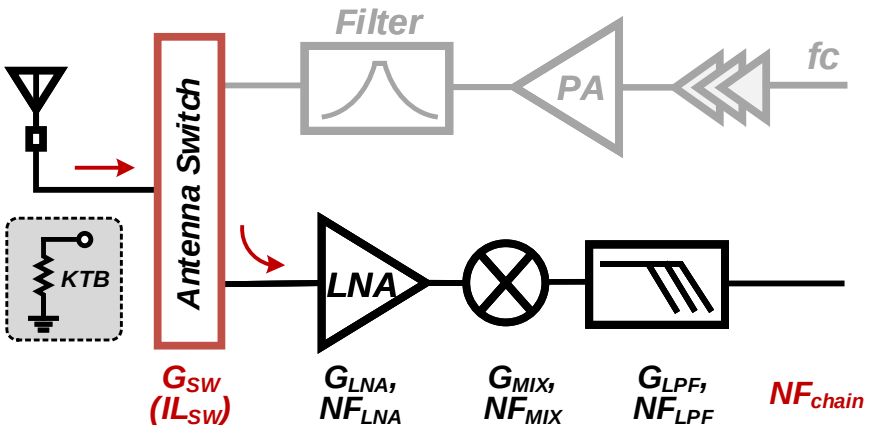


Figure 1.10: The simplified receiver model.

To maximize the sensitivity also the communication distance, the noise figure of the receiver chain should be minimized while a 10 dB SNR_{modem} is sufficient to the FSK receiver such as BLE. To achieve a -95 dBm receiver sensitivity, the upper limiter of the NF is estimated as:

$$NF_{chain} \leq -95(\text{dBm}) + 111(\text{dBm}) - 10(\text{dBm}) = 6(\text{dB}) \tag{1.7}$$

The total receiver chain noise figure should lower than 6 dB. That puts a stringent noise requirement of the radio frequency front-end (RF-FE) performances while a sufficient gain must be provided with low power consumption. Also, from the noise cascade equation using the receiver model shown in Fig. 1.10, the insertion loss of the passive component before the LNA will inevitably degrade the NF_{chain}, which can be expressed as:

$$NF_{chain} \approx IL_{SW} + NF_{LNA} + \cdots \tag{1.8}$$

The insertion loss of the antenna switch will be directly added to the total chain noise figure, while the noise figure of the LNA will dominate the total chain noise figure. Benefits from a more advanced CMOS process, the on-chip antenna can be realized with acceptable performance. However, the total noise figure including the LNA is approx to 5.5 dB as shown in [7], which is listed in Table 1.4. Also, the passive component like the inductor and transformer will dominate the RF front-end area, which occupies the main chip area ($\geq$ 60%). Therefore, the chip cost is inevitably increased. The transceiver link budget can be expressed as the following equation.

Table 1.4: SUMMARY OF THE T/R SWITCHES AND THE DESIGN TARGET.

	Target	[7]	[8]	[9]
Tech.	65nm	90nm	180nm	350nm
LC Resonator Switch	Yes	Yes	Yes	No
LNA/PA Co-design	Yes	Yes	No	No
VDD	1	1.3	0.6/1.8	3.3
TX Insertion Loss	<1*	<0.5	2.02/1.62	1.2
Filter/LNA Bypass	Yes/Yes	No/No	No/No	No/No
Return Loss (RX/TX, dB)	>15	>10	>10	>15
RX Isolation (dB)	>40	16	17.15	>15
LNA NF (dB)	<4*	5.5	N.A.	N.A.
P1dB (dBm)	>0	>30	>30	20.6
Total Ind. Number	<4	5	2	0
Area (mm^2)	<0.6**	N.A.	0.13**	N.A.

* Estimated.
** Integrated with LNA and PA.

$$LinkBudget = Max.RXsensitivity\,(\text{dBm}) - Max.TXPower\,(\text{dBm}) \tag{1.9}$$

The link budget indicates the maximum communication distance. Considering a TX with a maximum 10 dBm output power and an RX with a -95 dBm maximum sensitivity, the link budget can be calculated as -105 dB. To extend the communication distance, in other words, link budget, and also enhance the robustness in the room with obstructions, a high sensitivity receiver is required and thus, the insertion loss of the antenna switch should be seriously considered. The power consumption and the chip cost should also be taken into account. The design targets are listed in Table 1.4.

Another challenge comes from the large input power (-10 dBm in V5.2). However, a larger power handling capability can be robust in the communication with a nearby transmitter embedded large output power. The large input signal will saturate the LNA and desensitize the RX with generating inter-modulation, *e.g.,* 3rd-order inter-modulation distortion (IMD3), which degrade the SNDR ratio. The intercept point (IP) is used to evaluate the linearity performance while the input intercept point of the fundamental and 3rd-order harmonic (IIP3). To estimate the largest required IIP3 performance with the maximum input power, *e.g.,* -10 dBm, the following equation can be utilized.

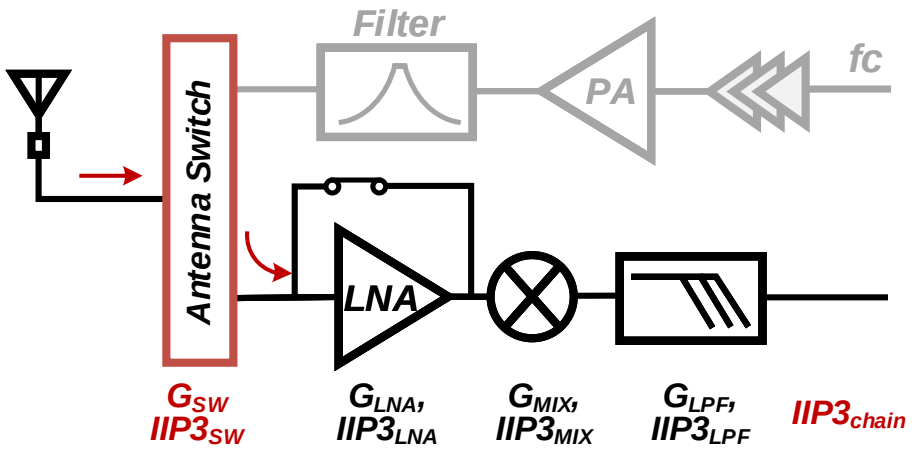


Figure 1.11: The simplified receiver model for IIP3 calculation.

$$\begin{aligned} IIP3_{maximum} &= Max.\,Input\,Power\,(\mathrm{dBm}) + \frac{SNR_{modem}}{2}\,(\mathrm{dB}) \\ &= -10+7 = -3\,(\mathrm{dBm}) \end{aligned} \tag{1.10}$$

For the receiver chain cascaded IIP3 estimation, the model shown in Fig 1.11 is utilized and the estimated IIP3 can be written as:

$$\frac{1}{IIP3_{\mathrm{RX}}} \approx \frac{1}{IIP3_{\mathrm{SW}}} + \frac{G_{\mathrm{SW}}}{IIP3_{\mathrm{LNA}}} + \frac{G_{\mathrm{SW}}G_{\mathrm{LNA}}}{IIP3_{\mathrm{MIX}}} + \cdots \tag{1.11}$$

From equation 1.11, the cascaded IIP3 will be dominated by the following stages, *e.g.,* LPF and VGA. To enhance its linearity and also the IIP3 performance, a large power budget is required while providing a low-gain path is also a selectable way to realize this large IIP3 requirement, as shown in Fig 1.11. As one of the most power-hungry part in the front-end, the LNA performances are quite important. The noise figure with integrated antenna switch should be minimized (<4 dB), while a large tunable gain range (>35 dB) should be realized, all with low power consumption (<0.6 mW).

Since introducing an LNA bypass route and antenna switch will degrade the minimum NF of the LNA, more strict performance of the antenna switch should be specified. Furthermore, the impedance matching condition has to be considered in the LNA bypass mode.

Another challenge for RX is coming from the ACR performances, as shown in Fig. 1.12. While the ISM is getting crowded with multiple devices, the RX's ACR performances

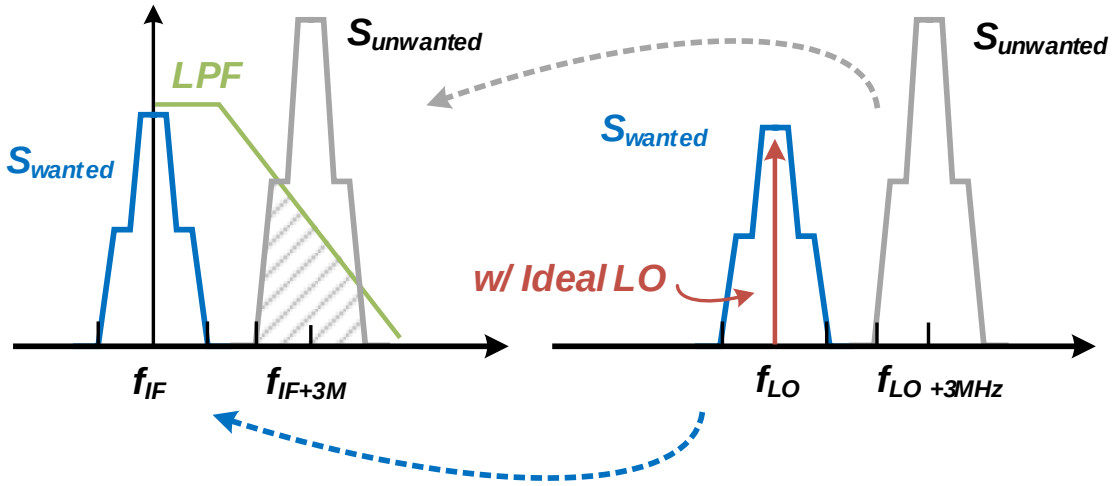


Figure 1.12: The simplified receiver model for ACR calculation using ideal LO.

also become more important. Considering the ACR performances at 1 MHz, 2 MHz, and 3 MHz, the 3 MHz has the most strict requirement due to the insufficient interference suppression from the analog baseband low-pass filter (LPF). For a conventional 4^{th}-order with a 500 kHz bandwidth, only 38 dB reinforced suppression (at 3 MHz, 62 dB suppression) available from the LPF compared with 1 MHz case (24 dB suppression). However, the 3 MHz specified ACR performance is 42 dB higher than the value specified at the 1 MHz. Higher-order filter implementation requires more power due to the more active transistors. Considering the non-ideal effect from the ADC and the front-end, a much higher suppression ratio from the LPF is required, *e.g.,* 4^{th}-order with a 500 kHz bandwidth, which has a 62 dB suppression. As we also noticed, only the ACR performance is specified with a -70 dBm input power case. That means the order of the LPF can be reduced with high input power, *e.g.,* a -20 dBm input power can just use one order LPF because of the sufficient large input signal compared with adjacent interference. This consideration provides us with ideas to reduce front-end power consumption according to the input power strength, *e.g.,* bypass some stages in the LPF.

The local oscillator, as one of the power-hunger part in the transceiver, has a negligible impact on the SNR performance because the level of the phase noise (PN) is much lower than the sensitivity (< 10 dB). However, the PN can be the critical issue of the ACR performance due to the reciprocal mixing, as shown in Fig 1.13.

The ideal PN performance has less influence on the in-band noise because the unwanted signal is only down-converted to the adjacent location and filtered by the LPF, as

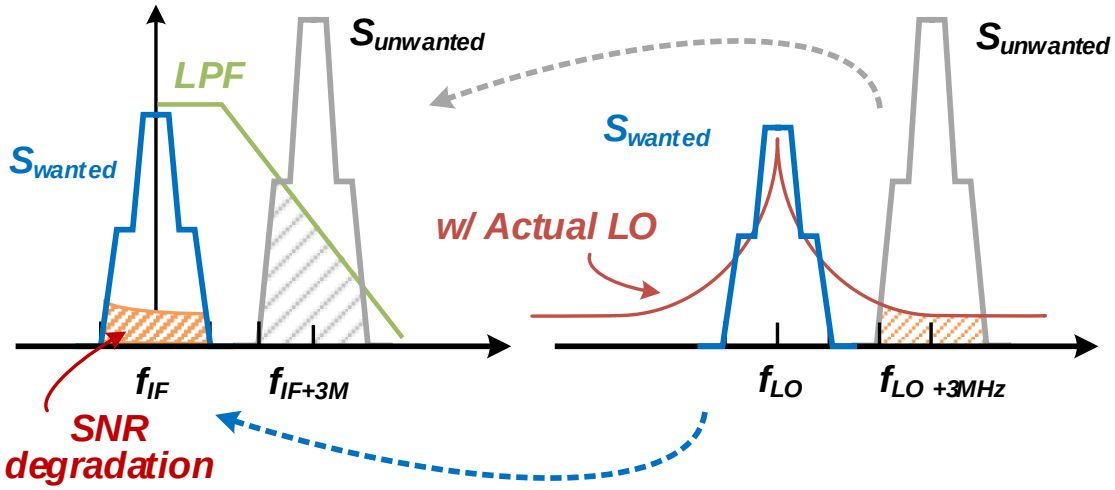


Figure 1.13: The simplified receiver model for ACR calculation using actual LO.

shown in Fig 1.12. In contrast, the non-ideal PN performances with noise skirt will down-convert the interference into the in-band, which cannot be filtered and finally causes the SNR degradation. Generally, the local frequency generator is a phase-locked loop (PLL), which implements an LC-type oscillator. The PN of the PLL at the adjacent channel where exists a large interference will contribute to the in-band noise. Because of this, the PLL PN performances and the spur performance have to be considered seriously. And the following equation can be utilized to calculating the minimum required PN based on the most stringent requirement.

$$\mathcal{L}_{\mathrm{PN,max}} \approx S_{\mathrm{wanted}} - S_{\mathrm{unwanted}} - SNR_{\mathrm{min}} - 10\log BW_{\mathrm{eff,noise}} \tag{1.12}$$

S_{wanted} : the wanted signal strength.
S_{unwanted} : the interference signal strength, *e.g.,* blocker at 3 MHz.
SNR_{min} : the required power ratio between the wanted signal and the down-converted interference.
$BW_{\mathrm{eff,noise}}$: the signal bandwidth to calculate the integrated power.

In the operation of PLL, there are some inevitable fractional spur or the reference spur (far from the adjacent because of the much higher reference frequency). These spurs will also degrade the SNR ratio due to the reciprocal mixing, while these spurs have much higher energy compared with the phase noise. At the same time, the maximum spur level can be estimated using the following equation, which is similar to equation 1.12.

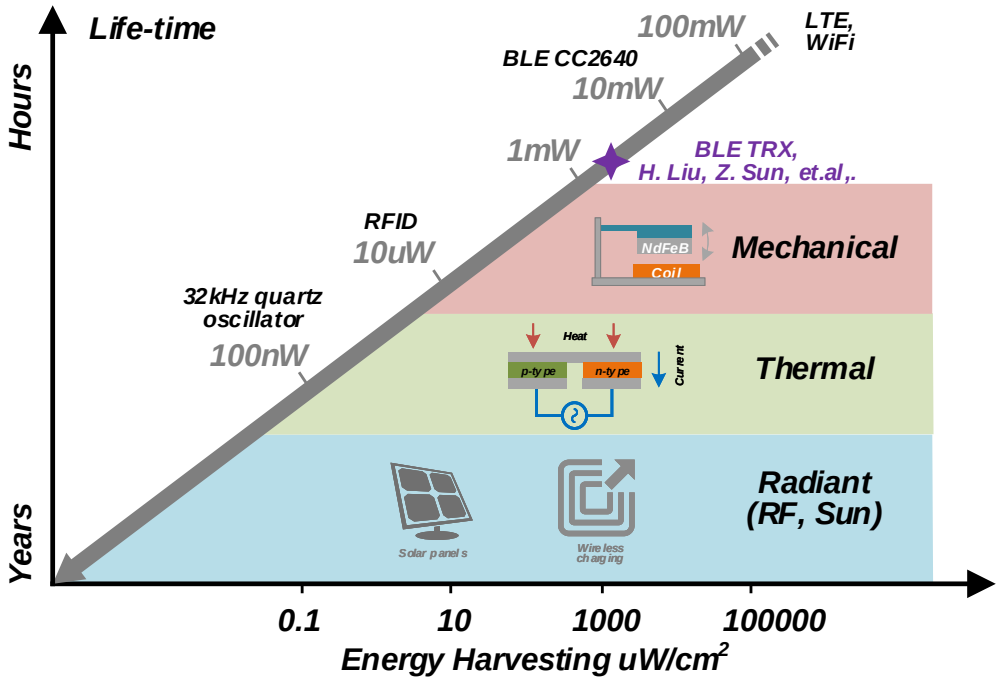


Figure 1.14: Power consumption for typical applications including BLE and power densities for various energy sources.

$$Spur_{\text{max},\geq 3\text{MHz}} \approx S_{\text{wanted}} - S_{\text{unwanted}} - SNR_{\text{min}} \tag{1.13}$$

Considering the desired signal level with -67 dBm under a -40 dBm blocker at 3-MHz offset, a LO noise performance of less than -99 dBc/Hz at 3-MHz offset with lower than -40 dBc spur level is strictly required. However, in the real application, multiple interferences may exist, and the noise contribution from other non-ideal components,*e.g.,* DC-DC converter, should also be considered. As a result, the phase noise performance lower than -110 dBc/Hz and a maximum spur ratio lower than -50 dBc is sufficient in the BLE transceiver design.

1.4 Long Life-Time and Easy Implementation

The power consumption will be mainly dominated by the TX and RX active power if multiple transmitting and receiving steps are required. After finishing the receiving and transmitting steps, the TRX will do some post-process and enter the sleep mode to save the power. A typical coin battery is compact for its size. However, the energy it contains is also limited by its size. For example, an SR44 alkaline coin battery contains energy of

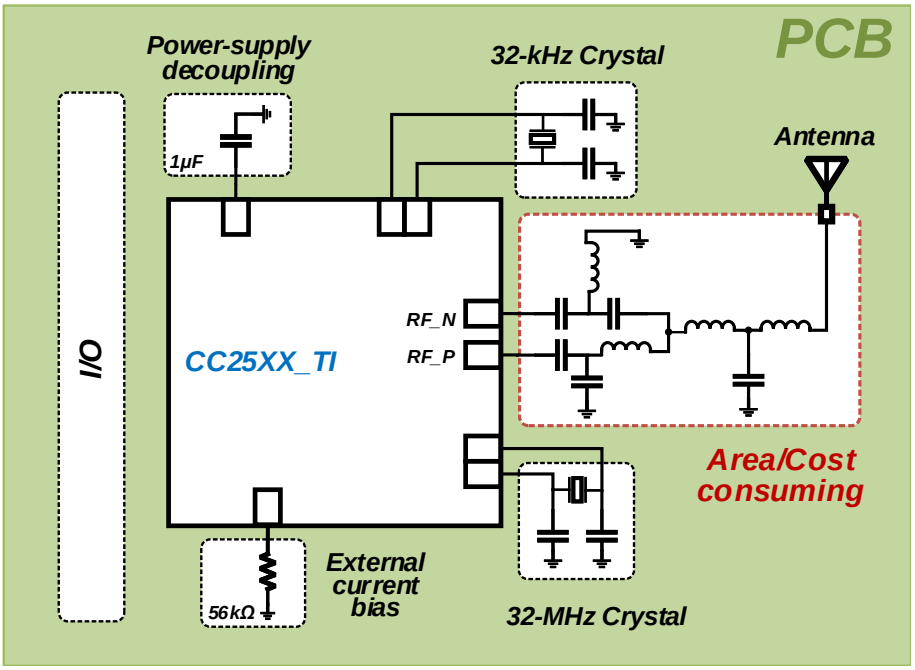


Figure 1.15: A typical application circuit shown in CC-series SoC data-sheet.

150 mAh. To breakthrough the battery capacity limitation, energy harvesting technology can be adopted.

As shown in Fig. 1.14, the power requirements of different applications, *e.g.,* WiFi application and the commercial Bluetooth application, and the power densities for various energy sources, *e.g.,* mechanical sources and the RF radiant source such as the wireless power transfer. Our previous BLE TRX work already achieved reported lowest BLE transceiver power consumption, which is also marked in Fig. 1.14. The source type which can be selected for the IoT application mainly depends on its application. There are some consideration including the target market, the energy efficiency, transmission strength and also the cost. What should be noticed here is that the cost should also include the consideration of the lifetime since the average cost can be reduced with an enhanced lifetime, as the following equation shows.

$$Cost_{\mathrm{AVG,year}} = \frac{Cost_{\mathrm{Design}} + Cost_{\mathrm{Chip}} + Cost_{\mathrm{Package}} + Cost_{\mathrm{PCB}} + \cdots}{Life\ Time} \tag{1.14}$$

Since several approaches can be utilized to enhance the lifetime, such as using the high energy density battery, energy harvested method (special application), and using the off-chip components to lower the loss. However, these methods just put the cost increase on the battery cost or the device/PCB cost. The PCB implementations, includ-

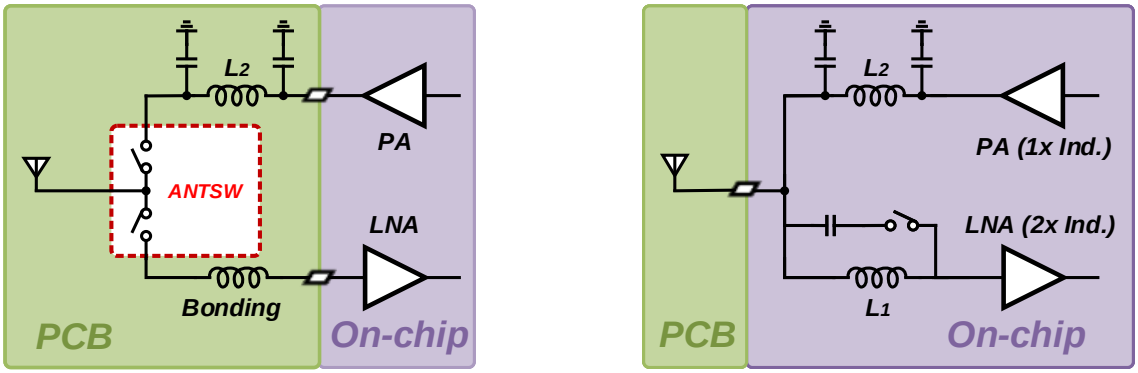


Figure 1.16: Previous of BLE works.

ing the BLE SoC, radio frequency input-output, and metal planar antenna, are shown in Fig 1.17. Through the off-chip component, *e.g.,* antenna switch, has better performance, *e.g.,* <0.5 dB insertion loss. The total cost may be increased due to the large PCB area and the cost from the off-chip components.

A typical PCB implementation using the commercial SoC (Texas Instruments CC-25XX [10]) is shown in Fig 1.15. Two crystal oscillators are implemented in this application circuit. One is the 32.768 kHz with an ultra-low power consumption, which is always on and works for the sleep timer and watchdog timer. Another one is the 32 MHz reference, and it is mainly for the RF operation, which can provide a much more accurate high-frequency reference. In this implementation, the passive components, except for the two crystal, is mainly used in the radio frequency port. As shown in Fig 1.15, the total passive components, *e.g.,* capacitors and inductors, for the antenna connection is nine while only six passive components and two crystal oscillators for other functions. Considering the normal price of the passive components, *e.g.,* 0.006 $ for each capacitor, the total cost for the antenna connection in the BLE SoC implementation is over 20% of the total PCB cost (without considering the cost for the soldering).

Another two BLE works are shown in Fig. 1.16. In [11], off-chip filters are required while two SMA connectors are embedded with the PCB to connect with two antennas. Otherwise, an off-chip antenna switch is required. The off-chip area is inevitably increased with more off-chip components, and it is difficult to make the BLE module become smaller due to the PCB size. The other one is from the Renesas [12]. The on-chip resonate switch avoids the off-chip antenna switch implementation. However, as we notice, the configurable notch filter implementation leads to the NF degradation due to the limited impedance from the TX path. Also, as we noticed, there is an additional one inductor in PA design and two inductors in LNA design, and the total on-chip inductor

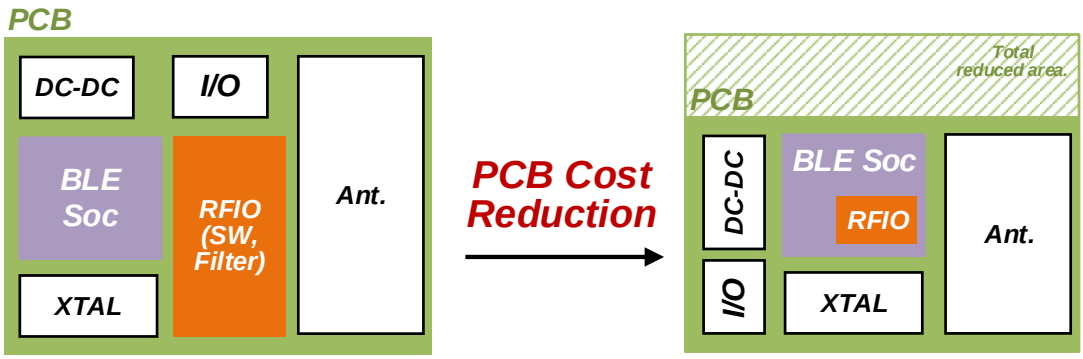


Figure 1.17: The concept of PCB cost reduction for BLE applications.

number is five, which inevitable increases the on-chip area and the cost. Since there is no LNA bypass route in this design, the LNA will still suffer from the large input power, and large power is required.

Since the application-specific integrated circuit (ASIC) cost includes the PCB cost and includes the die cost and the test cost (not considered in this thesis). These three costs cover most of the ASIC cost. To realize the mass deployment in a cheap way, *e.g.,* mesh network of sensors. The die cost should also be seriously considered and reduced. Since we can integrate the off-chip components using the on-chip method in a conventional way, as shown in Fig. 1.17. However, the size of the die area will inevitably increase. To maximum reduce the chip area and also the die cost, the passive components in the RFIO should be designed with reusable functions, especially the inductors for the impedance matching and the TX harmonic filtering, which takes most of the chip area, as shown in Fig. 1.18.

Meanwhile, a small and low-power BLE module, within a compact package size, is extremely attractive for disposable or highly integrated portable devices. That also means the die area should be minimized but with the whole functions embedded (without the need for the passive components), *e.g.,* on-chip antenna switch and harmonic filtering. Also, there are some area reduction techniques that can be implemented in the BLE transceiver design, *e.g.,* the digital phase-locked loop implementation which doesn't need a large on-chip filter. The transceiver structure also has to be seriously considered with a trade-off between the on-chip area and the target performances.

Hence, the main target for this thesis is to achieve remarkable power consumption (enhanced lifetime) and excellent performances (including the sensitivity, TX efficiency, ACR, and so on) within a lower overall cost, including the die cost and the PCB cost.

As discussed in Section 1.3, the main challenges remain in the antenna switch implementation, which should consider the RX NF, TX insertion loss, power consumption, and the on-chip area, and also the LO oscillator which should take the power and the PN

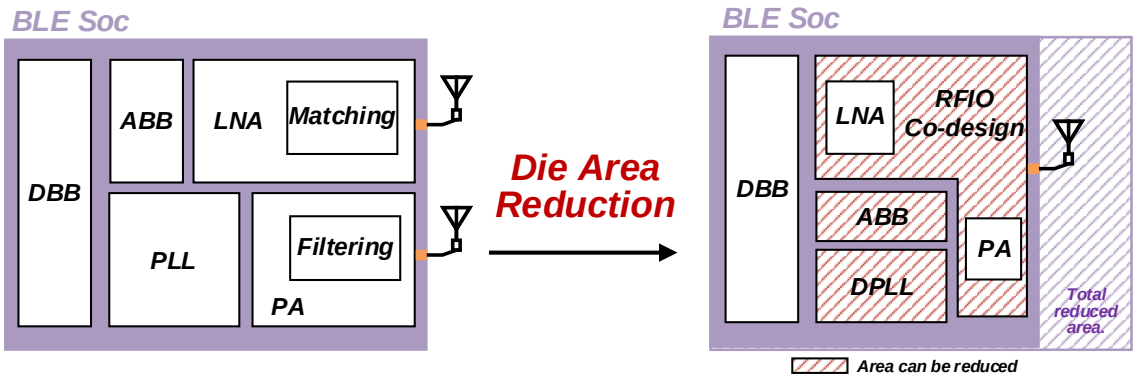


Figure 1.18: The concept of SoC area reduction for BLE applications.

performance into account. The detailed design target is listed in the following table 1.5 as the references in the design process.

1.5 Overview of the Thesis

The aim of this thesis is to investigate and achieve a fully integrated small-area and low-power RF front-end using advanced CMOS technology toward the future IoT technology. The thesis is organized as follows:

Chapter 1 begins with an overview of the background of the IoT and the different wireless standards for IoT applications. In this part, the importance of the BLE standard is discussed. Based on the newly released Bluetooth standard core specification V5.2, the important specifications have to be analyzed for transmitter and receiver, respectively. According to the analysis, the key performances of some building blockers and design targets are specified. Chapter 1 also analyzed the design challenges for the low-power and small-area BLE TRX design when considering the actual applications.

Chapter 2 introduces an ultra-low-power TF-based VCO for IoT applications. First, the VCO theory is revised, and some conventional VCO structures, typically low-power structures, are discussed. The impulse sensitivity function (ISF) is adopted to analyze the phase noise characteristics of oscillators. And the simulation method of the ISF function is organized and summarized. The proposed VCO achieves a -114.8 dBc/Hz PN at 1-MHz frequency offset with a 103 µW power consumption. A -193 dBc/Hz FoM is achieved at 2.6 GHz oscillation frequency. The low-power operation and large transistor size improve the flicker corner to 16 kHz. The low-flicker noise and good $1/f^2$ PN performance allow the open-loop operation in a maximum 17-ms packet length BLE transceiver. And thus, the power efficiency of the TX can be further improved with the implementation of the proposed VCO. The PGS embedded TF used in this work indicates that the lay-

Table 1.5: THE DESIGN TARGETS OF THE LC-VCO, DIGITAL PLL AND THE BLE TRANSCEIVER.

Parameters			Value
TX or RX	PLL Performances	PN@3MHz	-120 dBc/Hz
		Power	<1.5 mW
		Frac. Spur level	-50 dBc
	VCO	PN@1MHz	-110 dBc/Hz
		Power	<200 μW
		Tuning Range	2.1 GHz$\sim$2.7 GHz
		Flicker Corner	<50 kHz
RX	Sensitivity	Target	-90 dBm
	Maximum Input Power	Target	+10 dBm
	Packet Error Rate (Bit Error Rate)		30.8% (0.1%)
	Adjacent Channel Rejection	Fulfill	Yes
	Power		<3 mW
	Blocker	Fulfill	Yes
TX	Output Power	Maximum	0 dBm
		Minimum	-10 dBm
	FSK error	Maximum	<3 %
	Spectrum	Fulfill	Yes
	Off-chip Filter		No
	TX efficiency		>15%
TRX	On-chip Area		<1 mm^2

out can be realized with a smaller on-chip area. The core area of the proposed VCO is only 0.12 mm^2, as same as the transformer itself. To mitigate the PN degradation from the voltage ripple introduced by the DC-DC converter in battery-powered portable devices, a supply pushing reduction loop is embedded with the VCO while consuming no additional voltage headroom. The power consumption of this loop is also minimized to 40 µW, and the supply pushing is reduced to 2 MHz/V, resulting in a -50 dBc spur with 5 MHz sinusoidal ripples. This chapter also presents a good jitter performance and low power consumption injection-locked clock multiplier (ILCM) for IoT applications in 65-nm CMOS. A transformer-based ultra-low-power (ULP) LC-VCO is proposed to minimize the overall power consumption. The introduced capacitor feedback path boosts the VCO loop gain, and thus a robust startup can be obtained. The proposed transformer-based VCO achieves -115.1 dBc/Hz at 1 MHz frequency offset with a 97 µW power consumption, which corresponds to a -194 dBc/Hz VCO figure-of-merit (FoM). Thanks to the proposed low-power VCO, the total ILCM achieves 78 fs RMS jitter while consuming 210 µW power. A -269 dB FoM_{JP} of jitter and power is achieved by this proposed ILCM, and a -262 dB FoM_{JRP} is obtained while considering the 520 MHz input reference with multiplication factor equals to 5.

Chapter 3 presents a miniaturized Bluetooth Low-Energy (BLE) transceiver (TRX) for short-range Internet-of-Things (IoT) applications in 65-nm CMOS. An integrated Radio-Frequency Input-Output (RFIO) embedded with transmitter/receiver (TX/RX) switch function and on-chip impedance matching is proposed. A hybrid-loop TRX structure based on a wide-BW fractional-N digital phase-locked loop (DPLL) is implemented to achieve the maximum power reduction. A -94 dBm receiver sensitivity is achieved with 2.3 mW receiver (RX) power consumption while an RF receiving bypass route integration enhances the input power tolerance. The BLE transceiver delivers -6 dBm output power while consuming 2.6 mW and achieves 18.5% maximum TX efficiency at 0 dBm output power. Thanks to the RFIO with harmonic suppression, -56 dBc of 2^{nd}-order harmonic distortion (HD2) and -48 dBc of 3^{rd}-order harmonic distortion (HD3) suppression are achieved with 0.85 mm^2 on-chip area. This transceiver satisfied the BLE radio specification without the need for external filters and with low-power consumption, which enables minimum size and long lifetime modules.

Chapter 4 is the conclusions for the thesis and the presented studies. Finally, future works are discussed for further developing the presented researches in this thesis, such as the Bluetooth 5 TRX and the high-performance frequency generator. In the Bluetooth 5 TRX design, a current-reused ring oscillator based low-power transmitter design is introduced. And multiple modes of the combination of the LC-oscillator and ring oscillator are conceived to realize both low-power mode and high-performance mode, which are

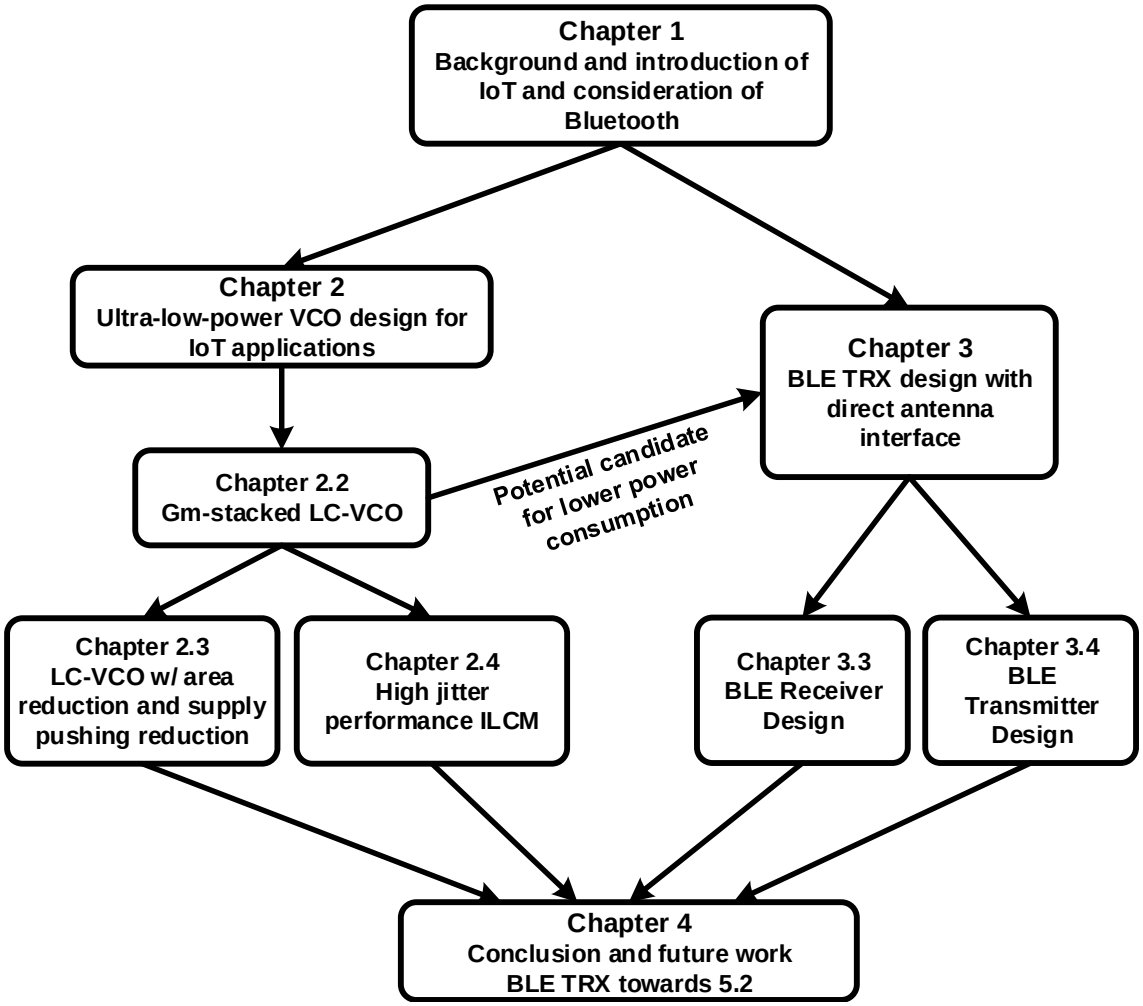


Figure 1.19: Measured return loss in TX and RX.

specified in a new standard.

The structure diagram of this thesis is shown in Fig. 1.19. The techniques presented in Chapter 2 can be potentially applied in BLE transceiver designs to reduce the on-chip area and power consumption. All the techniques proposed in this thesis can be candidates for the next generation BLE TRX transceiver design towards 5.2. The proposed low-power VCO techniques can achieve sufficient phase noise performance, which can satisfy the high output power required TX design. The injection locking techniques can also be potentially used in the TX modulation, in which the spur emission issue should be solved. A similar small-area RFIO design can also be applied in the v5.2 TRX with the reduced on-chip area and off-chip components.

As we know, the whole Bluetooth transceiver is a big system that includes a controller, *e.g.,* physical layer and link layer, host which includes such as logical link control and security manager, and also the applications. In this thesis, a part of the physical layer is

introduced, which also includes many circuits. Some improvements and innovations in the part are introduced and elaborated. I hope that these contents can inspire the future generations about their work and play a small but practical role in the next applications coming soon.

Chapter 2

Ultra-Low-Power Transformer-based LC-VCO

2.1 Low-Power LC-VCO and Implementation in PLL Design

In recent years, internet-of-things (IoT) has attracted a lot of attention, and in which the wireless transceiver plays a demand those transceivers with the embedded low-power operation to extend its lifetime with a limited battery capacity [11][13], and miniaturized modules to realize high integration and lower costs [14]. As an essential component of the frequency synthesis part in wireless transceivers, VCO is always power-consuming [15] and sensitive to DC supply variation. The ring oscillator is attractive to its small area occupation, but the poor phase noise (PN) performance limits its application on the high standard transceivers. Also, it is hard for the power of ring oscillators to be lower than 1 mW at several GHz applications while keeping a sufficient PN performance [16]. LC-VCO, which has much better PN performance and lower power consumption, is suitable for some popular wireless standards, such as Bluetooth [4]. However, the sizable on-chip inductor size is contrary to the miniaturization of the transceiver. As introduced in one of the Bluetooth low-energy (BLE) transceiver (TRX) design [15], -99 dBc/Hz at 3-MHz offset is required for a phase-locked loop (PLL) when considering the most stringent ACR performance. Thus, an LC-VCO, which can achieve lower than -110 dBc/Hz PN, is sufficient for BLE standard with enough margin. Meanwhile, the open-loop operation of VCO can be beneficial in saving TX power without any budget for other blocking of PLL, which requires the VCO to have a low-flicker corner and a better $1/f^2$ PN performance [17].

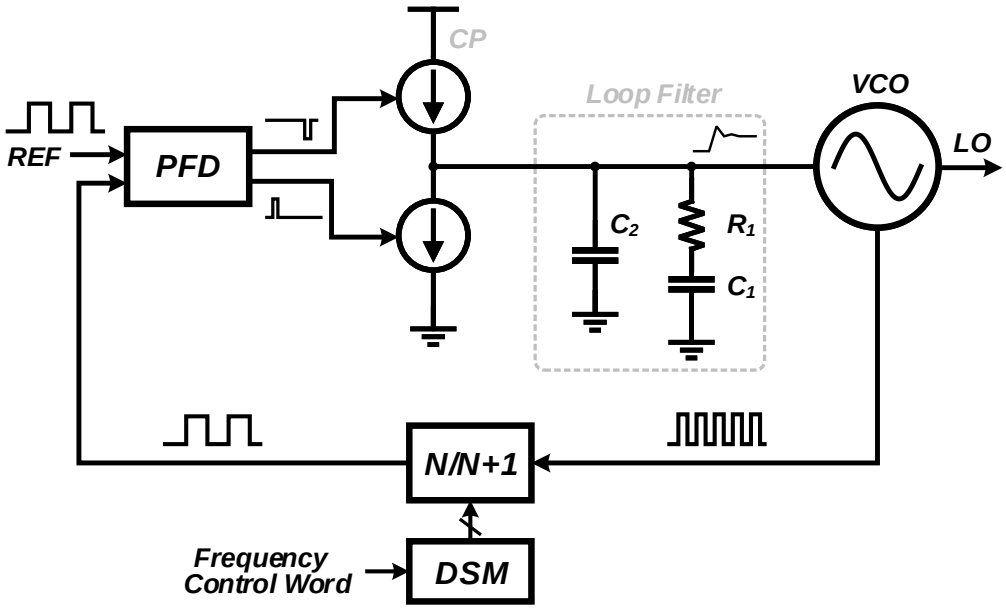


Figure 2.1: Structure of the traditional charge pump based PLL.

2.1.1 LC-VCO in Conventional PLL Design

In a transceiver, the phase-locked loop is the critical component that provides the precise frequency (phase) in radio frequency for the signal up/down conversion. The LC-VCO can provide a radio frequency signal. But due to its frequency instability and phase uncertainty, the LC-VCO's RF signal can't be used directly. The PLL is such a kind of feedback loop that utilizes a reference signal to correct the LC-VCO's LC-VCO's output phases, the PLL synchronizes VCO frequency, *e.g.,* 2.4 GHz, to input a reference frequency, *e.g.,* 40 MHz, through feedback. To understand the role of VCO, let's briefly review the conventional analog type PLL (charge pump based PLL, CPPLL). The CPPLL, comparing with the emerging digital type PLL, still has better phase noise performances with a simple structure but a larger on-chip area. We can derive a similar structure from the traditional analog PLL and implement it in a digital circuit. The traditional CPPLL is shown in Fig 2.1.

The phase/frequency detector (PFD) compares phase differences between the feedback signal from the multi-modulus divider (MMD) and the external reference. And the PFD will control the upper and the lower current source to charge or discharge the current into the loop filter by using pulses with short pulse width, which represents the phase error. The charging/discharging current will be converted into a voltage signal in the loop filter, and the output voltage will control the VCO oscillation frequency as a correction signal. For example, assuming the VCO has a leading phase compared with the reference signal. The PFD will convert it to a negative control voltage to make the VCO slow down,

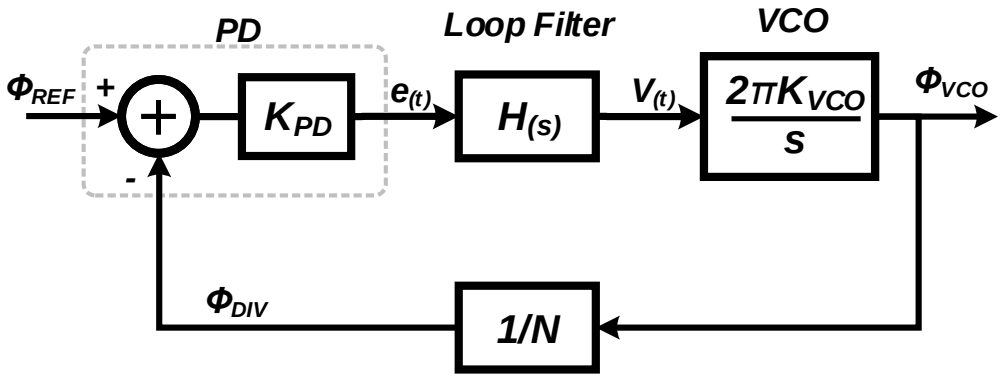


Figure 2.2: The frequency-domain model of the traditional charge pump based PLL.

and finally, the phase between the VCO and the frequency can be synchronized.

Since the time-domain model of the PLL is introduced, the frequency-domain model (same as Laplace-domain) can be expressed as shown in Fig. 2.2. Since the VCO output frequency can be expressed by using the VCO gain K_{VCO} (in Hz/V) multiplied with the voltage control signal V_t. The output phase of the VCO can be expressed by integrating the output frequency. Thus, we have

$$\Phi_{\mathrm{VCO}} = \int_{-\infty}^{t} 2\pi K_{\mathrm{VCO}} V_{\tau} d\tau \tag{2.1}$$

According to 2.1, the transfer function of the VCO from its input to the output in the frequency domain can be expressed as $\frac{2\pi K_{\mathrm{VCO}}}{s}$. While considering the transfer function of the MMD, PFD, and also the loop filter. The forward gain of $K_{Forward}$ the CPPLL without feedback can be written as:

$$K_{\mathrm{Forward}} = K_{\mathrm{PD}} \cdot H_{(\mathrm{s})} \cdot \frac{2\pi K_{\mathrm{VCO}}}{s} \tag{2.2}$$

Meanwhile, the loop gain (with feedback gain $G_{\mathrm{FB}} = \frac{1}{N}$) can be expressed as:

$$\begin{aligned} G_{Loop} &= K_{\mathrm{Forward}} \cdot G_{\mathrm{FB}} \\ &= K_{\mathrm{PD}} \cdot H_{(\mathrm{s})} \cdot \frac{2\pi K_{\mathrm{VCO}}}{s} \cdot \frac{1}{N} \end{aligned} \tag{2.3}$$

From the forward gain 2.2 and the loop gain 2.3, the transfer function of the CPPLL can be simplified as:

$$\begin{aligned} G_{close-loop} &= \frac{K_{\text{Forward}}}{1+G_{Loop}} \\ &= \frac{K_{\text{PD}} \cdot H_{(\text{s})} \cdot \frac{2\pi K_{\text{VCO}}}{s}}{1+K_{\text{PD}} \cdot H_{(\text{s})} \cdot \frac{2\pi K_{\text{VCO}}}{s} \cdot \frac{1}{N}} \\ &= \frac{2\pi K_{\text{PD}} K_{\text{VCO}} H_{(\text{s})} \cdot N}{sN + 2\pi K_{\text{PD}} K_{\text{VCO}} H_{(\text{s})}} \end{aligned} \tag{2.4}$$

To simplify the close-loop transfer function analysis, the K_{PD} and the divider ratio N are specified to 1. The transfer function of the CPPLL can be re-written as:

$$G_{close-loop} = \frac{2\pi K_{\text{VCO}} H_{(\text{s})}}{s + 2\pi K_{\text{VCO}} H_{(\text{s})}} \tag{2.5}$$

The number of the pole in the close-loop function equation 2.5 will decide the type of the feedback control system. If there is only one pole, which means there is no pole from the loop filter $H_{(\text{s})}$ and the only pole in the denominator is from the VCO, we call this type of PLL is Type-I PLL. Type-I PLL shows better responding speed and, in other words faster initial frequency acquisition. However, its noise performance is not as good as the Type-II PLL, which has two poles in the denominator (another introduced by C_2 in loop filter), as the loop filter shown in Fig. 2.1.

$$\begin{aligned} H_{(\text{s})} &= \frac{1}{sC_2 + \frac{1}{\frac{1}{sC_1} + R_1}} \\ &= \frac{sC_1R_1 + 1}{s^2C_1C_2R_1 + sC_1 + sC_2} \end{aligned} \tag{2.6}$$

The static phase error in Type-II PLL is zero, and this type of PLL performs a better noise filtering capability, which results in a better phase noise performance. What should be noticed in the traditional analog PLL design, the loop filter will occupy a large on-chip area due to the huge capacitance value, which is a trade-off with the noise performance. Through the noise from the loop filter will experience the 1^{st} order low/bandpass filter characteristic (noise transfer function, determined by is there a pole in the filter). To mitigate the kT/C noise (from capacitor) and thermal noise (from resistor) in the total noise contribution in a narrow-band PLL design, the resistance can't be very large that results in a much larger capacitor size (Comparable with inductor area), which can't benefit from the scaled and more advanced process.

The VCO noise contribution in the traditional PLL design will experience a 2^{nd}-order

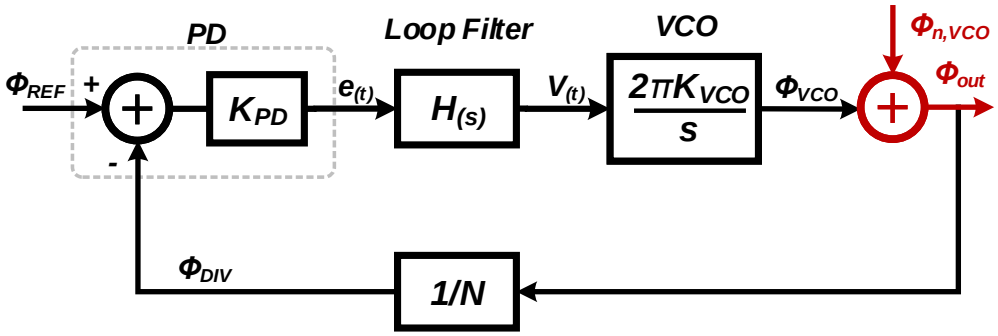


Figure 2.3: Frequency-domain model of the VCO noise contribution in traditional charge pump based PLL.

high pass filter characteristic, and the noise transfer function of the VCO can be written as:

$$\begin{aligned}\frac{\Phi_{OUT}}{\Phi_{n,VCO}} &= \frac{K_{\text{Forward}}}{1+G_{Loop}} \quad \text{in this case } K_{\text{Forward}}=1 \\ &= \frac{1}{1+\frac{K_{\text{PD}}\cdot H_{(s)}\cdot 2\pi K_{\text{VCO}}}{Ns}} \\ &= \frac{s}{s+\frac{K_{\text{PD}}\cdot H_{(s)}\cdot 2\pi K_{\text{VCO}}}{N}}\end{aligned} \tag{2.7}$$

In which, a simple loop filter $H_{(s)} = \frac{K_{\text{LF}}}{s}$ is considered with only one integrator instead of a complex transfer function, which is shown in equation 2.6. Thus, the noise transfer function of the VCO can be re-written as:

$$\frac{\Phi_{OUT}}{\Phi_{n,VCO}} = \frac{s^2}{s^2+\frac{K_{\text{PD}}\cdot K_{\text{LF}}\cdot 2\pi K_{\text{VCO}}}{N}} \tag{2.8}$$

The noise transfer function 2.8 in of the VCO shows a 2^{nd}-order high pass filter characteristic. While the noise of the other component, *e.g.,* reference, PFD, and the loop filter, will experience low-pass or band-pass characteristics. That also means noise out of the PLL bandwidth will mainly be determined by the VCO noise.

The CPPLL has been the most popular PLL architecture because of its good phase noise performances and robust implementation. CPPLL already achieve high performances and a good figure of merit (FoM). However, with the process scaling down, the digital process has more advantages in the calibration integration and the fully synthesizable circuit designs, which can be configured very quickly. Typically, the digital circuit like the digital filter can be easily realized in a much smaller area than the analog one

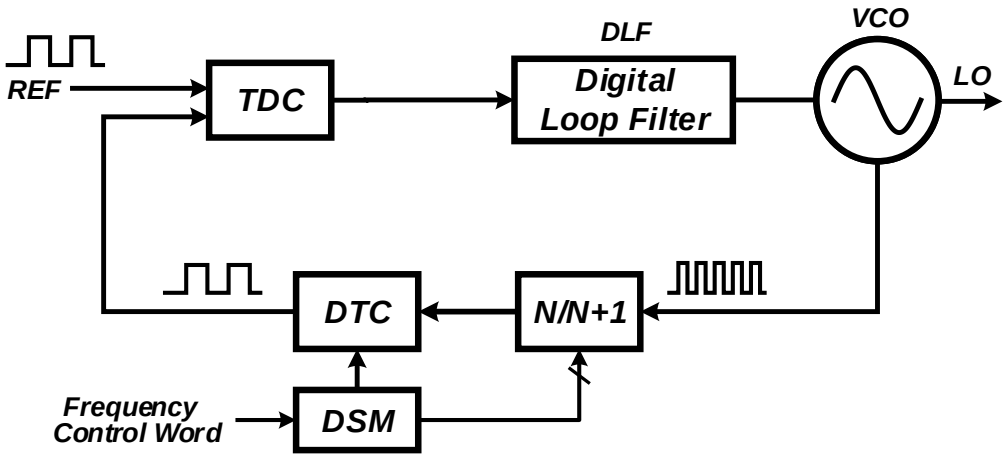


Figure 2.4: Structure of the digital phase-locked loop.

consisting of large capacitors. Also, the digital signal processing techniques can be applied in the digital phase-locked loop design, which makes the DPLL has more complex functions and comparable performances. To investigate the VCO noise in the DPLL, one conventional DPLL mode is shown in Fig. 2.4.

In the conventional structure of the DPLL, a time to digital converter is utilized to detect the phase difference between the feedback signal from the divider and the reference, which plays the same role as the PFD in the CPPLL. Generally, a counter which counts at each VCO cycle can be utilized to find the frequency error, *e.g.,* the counter based frequency locked loop. However, the phase information within one VCO cycle can't be extracted because the resolution of the integer counter is limited to one VCO cycle. Thus, a counter with a much smaller phase detector should be utilized to find the phase information instead of just using a counter. This structure also uses the delta-sigma modulator (DSM) and a multi-modulus divider (MMD) at the feedback path similar to the CPPLL. The FCW is over-sampled by the reference clock and input into DSM. The output of the DSM is modulated into the same length of the MMD control bits. To realize the fractional part, the modulated output of the DSM will dither the divider ratio of the MMD, *e.g.,* 60 and 61. Therefore, the average value of the divider ratio, *e.g.,* 60.5, should equal the integration of the FCW after many reference cycles.

Firstly, we consider the DPLL without the DTC, which eliminate the quantization error from the MMD operation in fractional mode. If the phase from the MMD doesn't align with the input reference, the TDC will produce a digital code that corresponds to the phase difference. The digital loop filter will filter this digital code and adjust the digital controlled oscillator phase. This operation is similar to the phase control in the CPPLL. The option of the TDC works as the phase error detector, which is the same as the PFD and the charge pump.

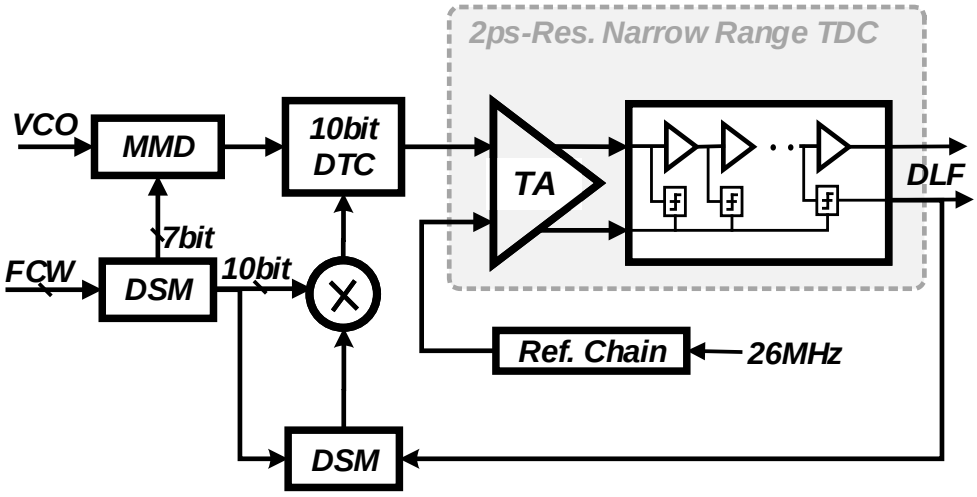


Figure 2.5: The implementation of DTC and narrow-range TDC.

In the counter-based DPLL case, the TDC range should be equal to the one DCO cycle. Otherwise, a large fractional spur will appear if there is any mismatch between the TDC range and the DCO cycle. In the divider-based DPLL structure, since there is no DTC that mitigates the MMD quantization noise, the TDC range should be larger than one DCO cycle (1^{st}-order DSM case), which needs a quite large range with a fine resolution. With a higher-order DSM implementation, the TDC range also needs to be enhanced, which leads to a dramatic increase in power consumption. Also, both the TDC and the counter will work in the DCO cycle without the divider, which consumes much power. In the divider-based structure, only the first stage of the MMD works in the DCO frequency, which saves much power.

Since the TDC range should be quite large, also both linearity and resolution are important for a low fractional spur and in-band phase noise performance. The divider-less structure requires a much large TDC power, and it is not applicable in the low-power frequency synthesizer design. Since we notice MMD works as an integer phase integrator, which introduces a large quantization error. Suppose MMD can work as a fractional integrator with a fine resolution, the TDC range can be dramatically reduced, which saves much power. Since a digital to time converter (DTC) is inserted in the feedback path after MMD, a fractional integrator with fine resolution can be realized, which is shown in Fig. 2.4. The quantization error from MMD can be reduced to several times of the DTC resolution, which results in a huge TDC range reduction (1 bit TDC, a latch-based BBPD can be applied). However, to exactly realize the fractional divider operation with a fine resolution, the DTC tuning range must be calibrated as same as the DCO cycle. If the DTC range (according to the DTC control code from the DSM) is larger than the DCO cycle, the resolution of DTC will be degraded. If the DTC range is less than the

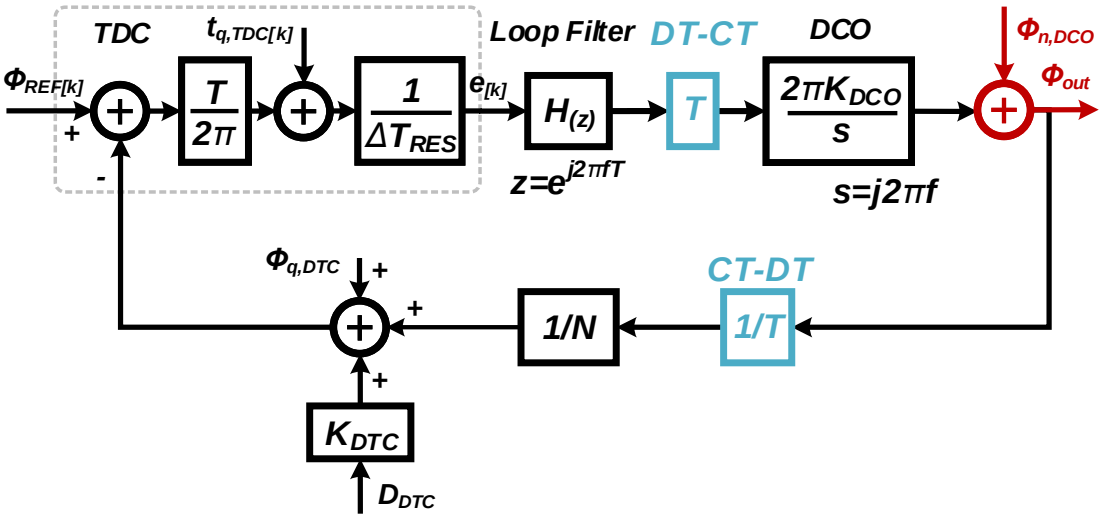


Figure 2.6: Digital PLL modeling with DCO noise contribution.

DCO cycle, the TDC range must be enlarged to cover the remaining phase difference. To realize this, an LMS algorithm [18] can be utilized by calculating the correlation of TDC output and DTC control code, which is shown in Fig. 2.5.

In the conventional DTC design, the resolution of DTC can be reduced to lower than 1 ps with a more than 600 ps range (1.5 times DCO cycle) with lower than 100 µW power, which is sufficient in the low-power design such as BLE. With assistant from the DTC, the TDC range can be reduced, and a time-amplifier (TA) can be implemented to achieve a smaller equivalent TA resolution, which leads to low in-band phase noise. As shown in Fig. 2.5, the flash-type TDC is the most commonly used in the low-power design with advanced technology. With a delay chain which consists with multiple buffer cell in a standard digital library, analog phase interpolation is generated and used to compare with another path input signal (reference signal). The leading phase will generate the "1" code, while the lagging phase will generate the "0" code. With a thermal to binary decoder, the phase information between the two input signals can be detected, which a conventional linear gain (step). The resolution and the linearity of the flash-type TDC are limited to the delay of each buffer cell and the mismatch between each buffer. To further improve the equivalent resolution, as mentioned, a TA can be utilized. And because the total range of the TDC is narrow, the linearity introduced by the mismatch of the cells can be ignored, which is much smaller than the resolution.

The compromise between power consumption, linearity, resolution, and noise performances should also be seriously considered for DTC design. There are several types of DTC, such as the ring-oscillator based DTC, variable-slop DTC, and the constant-slop DTC. The variable-slop and constant slop DTC have better resolution and noise perfor-

mances with lower power consumption. Because of the finite gain from the comparator in the DTC, the output delay will have code-dependence due to the different raising slope rate. The code-dependent delay is the major nonlinearity of the variable DTC. However, in the constant-slope DTC, the raising slope rate is always the same, while the charge starting point is determined by the pre-charge voltage. Thus, the code-dependent nonlinearity is removed. Still, there is a trade-off between the jitter performance (large current with large capacitance required) and the power consumption (power consumption from the current source) in the conventional constant-slope DTC.

To understand the noise contribution of the DCO in the DPLL design, the same analysis method is adopted as in the CPPLL. The model shown in Fig. 2.6 is utilized to analyze the DCO noise contribution in the digital PLL design.

$$\begin{aligned} H_{(n,DCO)} = \frac{\Phi_{OUT}}{\Phi_{n,DCO}} &= \frac{K_{\text{Forward}}}{1+G_{Loop}} \quad \text{in this case } K_{\text{Forward}} = 1 \\ &= \frac{1}{1+\frac{T}{2\pi}\cdot\frac{1}{\Delta T_{RES}}\cdot H_{(z)}\cdot T\cdot\frac{2\pi K_{\text{DCO}}}{j2\pi f}\cdot\frac{1}{N}\cdot\frac{1}{T}} \\ &= \frac{1}{1+\frac{1}{\Delta T_{RES}}\cdot H_{(e^{j2\pi fT})}\cdot T\cdot\frac{K_{\text{VCO}}}{2\pi jf}\cdot\frac{1}{N}} \end{aligned} \tag{2.9}$$

The output of the filtered DCO noise can be calculated with the derived noise transfer function and the original DCO noise using the following equation.

$$\begin{aligned} PN_{(DCO,DPLL)} &= H^2_{(n,DCO)}\cdot PN_{(DCO,Original)} \\ &= (\frac{\Phi_{OUT}}{\Phi_{n,DCO}})^2\cdot PN_{(DCO,Original)} \end{aligned} \tag{2.10}$$

Since we notice the DCO noise transfer function in DPLL is a high-pass function with a high-frequency gain of 1. That also means the PLL loop cannot filter the VCO noise at the high-frequency offsets, *e.g.,* 5 MHz. However, an RMS jitter is usually integrated from low frequency (*e.g.,* 1 kHz) to high frequency (*e.g.,* 40 MHz). The unfiltered DCO noise will dominate the total RMS jitter if the noise of DCO is not good enough. As shown in Fig. 2.7, noise contributions of DPLL with a -110 dBc/Hz @1 MHz DCO are shown. To show the effects of different phase noise from the DCO, a -100 dBc/Hz @1 MHz DCO is adopted while keeping other parameters the same, as shown in Fig. 2.8.

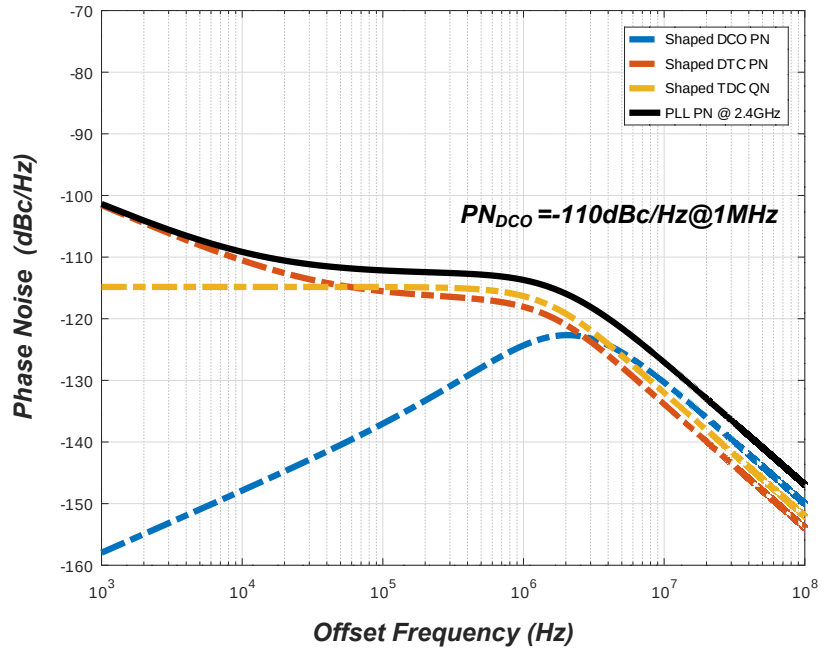


Figure 2.7: DPLL noise contribution from each component (PN_{DCO} = -110 dBc/Hz @1 MHz).

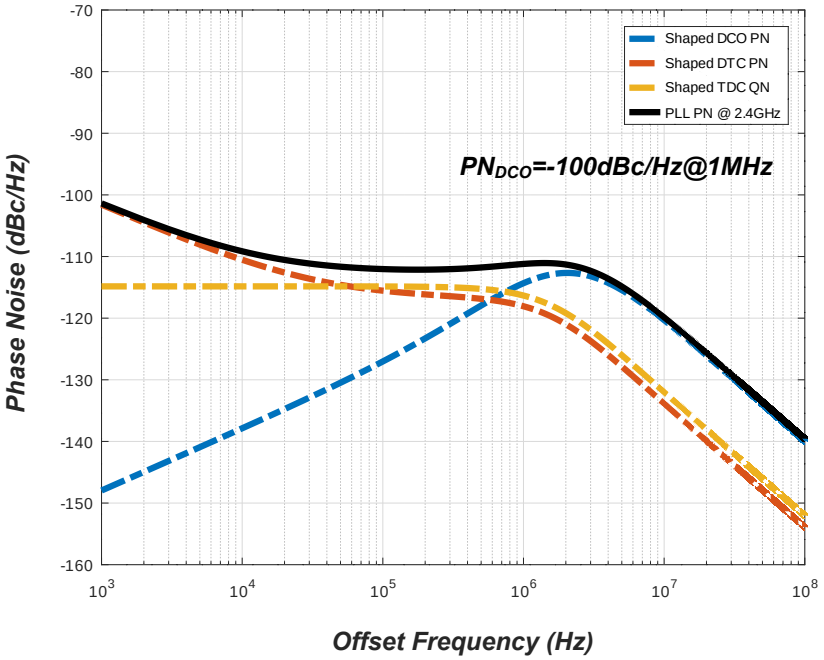


Figure 2.8: DPLL noise contribution from each component (PN_{DCO} = -100 dBc/Hz @1 MHz).

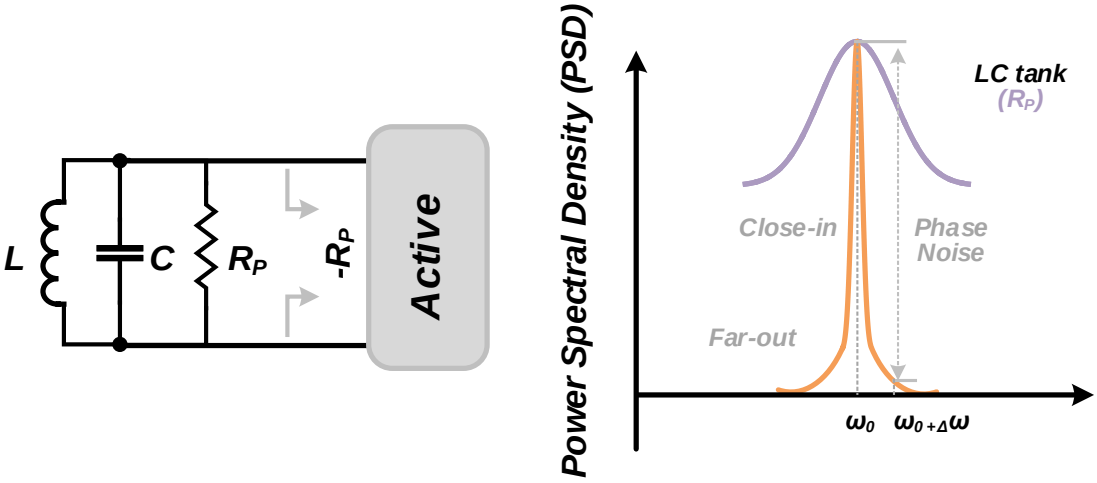


Figure 2.9: LC-VCO model and its power spectral density.

2.1.2 Phase Noise in LC-VCO

After understanding the VCO phase noise contribution in PLL designs, the fundamental of the VCO phase noise has to be reviewed. Understanding the noise contribution in the PLL and the VCO noise mechanism will help us design a low-power VCO that meets noise requirements.

There are mainly two types of VCO in radio frequency generation. One is the ring oscillator, which typically has a moderate phase noise performance, *e.g.,* >-100 dBc/Hz at 1 MHz offset, which is insufficient in the BLE transceiver design (discussed in section 1.3). Another type is the LC-VCO, which consists of an LC parallel tank and active devices (negative resistance), as shown in Fig. 2.9. The power from the active devices will be injected to the tank to compensate for the loss in the non-ideal LC tank. In the steady-state, the loss in the LC-tank from the R_P will be canceled (balanced) by the active device with negative resistance $-R_\mathrm{P}$.

To understand the operation of the VCO, firstly, the start-up condition should be investigated. Since the cross-coupled transistors provide negative resistance $-2/g_{m0}$. The g_{m0} is determined by the process and the bias current. Mathematically, to satisfy the start-up oscillation, the value of the $-2/g_{m0}$ can be selected as the same as the LC tank impedance R_P, which just exactly compensates the energy loss. However, to realize a robust start-up, the negative resistance g_{m0} much large than the minimum value, *e.g.,* $g_{m0} = 3g_{m0,min}$. Also the product of the tank impedance R_P and g_{m0} is defined as the excess gain, as shown in following equation.

$$G_\mathrm{X} = g_{\mathrm{m0}} \cdot R_\mathrm{P} \tag{2.11}$$

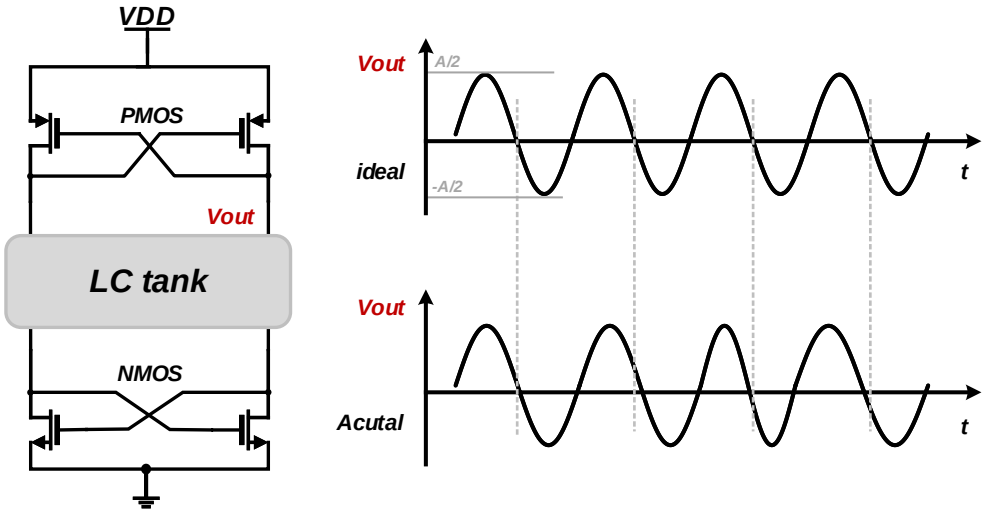


Figure 2.10: Output waveform of the LC-VCO in ideal case and actual case.

Since the excess gain G_X has a positive correlation with the flicker noise and also a large g_{m0} will lead to the transistors work in the triode region (degrade phase noise performance), the selection of the g_{m0} should be careful to satisfy the oscillation condition and to pursue a good phase noise performance.

The phase noise of the VCO is defined in the frequency domain, while the time-domain model of the VCO, as shown in Fig. 2.10, can be expressed as:

$$V_{out} = Acos(\omega_0 t + \phi(t)) \tag{2.12}$$

where the A is the oscillation amplitude, and ω_0 is the center oscillation frequency, which is equal to the frequency with maximum parallel impedance (ideal case). Here, $\phi(t)$ is a small random phase variation in the period, and commonly we called this $\phi(t)$ as the "phase noise". Since the phase variation $\phi(t)$ is a small value ($\ll 1^\circ$), the equation of the output waveform can be re-written as:

$$V_{out} = Acos(\omega_0 t) - A\phi(t)sin(\omega_0 t) \tag{2.13}$$

From this equation, we can find that the spectrum of the phase variation is translated into the center frequency ω_0. We can also guess that the closer to ω_0 will have the higher the spectral power density. To measure the purity of the oscillation, the noise power in a 1-Hz unit bandwidth at an offset frequency $\Delta\omega$ is considered and divided by the carrier power. The divided result in dBc/Hz is written as:

$$\mathcal{L}_{(\Delta\omega)} = 10\log_{10}\left(\frac{\text{Noise Power in 1 Hz Bandwidth at } \Delta\omega \text{ offset}}{\text{Carrier Power}}\right) \tag{2.14}$$

According to the LC tank impedance at an offset frequency $\Delta\omega$,

$$Z_{(\omega_0+\Delta\omega)} \approx j \cdot \frac{\omega_0 L}{2\frac{\Delta\omega}{\omega_0}} \tag{2.15}$$

By utilizing this equation, the noise power at the $\Delta\omega$ can be calculated, and the phase noise can be written using the noise power divided by the signal power, which is

$$\mathcal{L}_{(\Delta\omega)} = 10\log_{10}\left[\frac{2kT}{P_{\text{sig}}} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}^2\right)\right] \tag{2.16}$$

According to this basic equation [19], experimentally observed phenomena are added to the equation. That's the famous Leeson's phase noise model, which is written as:

$$\mathcal{L}_{(\Delta\omega)} = 10\log_{10}\left[\frac{2kT}{P_{\text{sig}}} \cdot \left(1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{2.17}$$

Q: is defined as the loaded quality factor of the tank, which is expressed as $Q = R/(\omega_0 L) = 1/(\omega_0 GL)$ (R/G represents the equivalent resistance of the transistors/transconductance).
k: is Boltzmann's constant.
T: is the absolute temperature in Kelvin.
P_{sig}: signal power in the tank at the desired frequency.
ω_0: oscillation frequency.
$\Delta\omega_0$: offset frequency.
$\Delta\omega_{1/f^3}$: is the boundary between the $1/f^(2)$ region and $1/f^(3)$ region.

From this equation, the main difficulty in VCO design is that the loaded tank quality factor Q and the signal power in tank P_{sig}. To enhance the Q, the current has to be increased (in other words, increase transconductance G with smaller inductance L) while the power loss in the tank should be minimized. In the low-power LC-VCO design, the focus is on how to achieve larger tank impedance and sufficient g_m to realize a robust start-up and how to maintain the phase noise performance with a limited current (since the L has to be large to provide enough impedance and g_m is limited by the current, the only thing we can do is try to improve the P_{sig} with the limited power). According to the Leeson's equation, the oscillator FoM can be derived as:

$$FoM = \mathcal{L}_{(\Delta\omega)} - 20\log_{10}\frac{\omega_0}{\Delta\omega} + 10\log_{10}P_{\text{DC}} \tag{2.18}$$

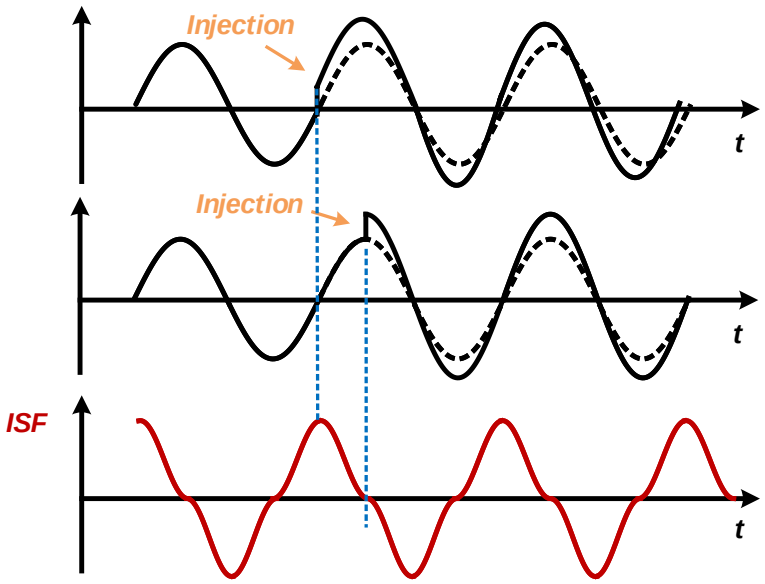


Figure 2.11: Injection current at different phases in the oscillator.

ISF Function and Simulation Method

Since the impulse sensitivity function (ISF) allows the designer to estimate the phase noise coming from a specified noise source and also plays a guiding role in noise optimization, the conventional ISF simulation methods, which based on the transient simulation, show difficulties in the suitable current pulse selection (large current pulse will result in a wrong result and too small current pulse will be affected by the numerical error). Also, the conventional way is time-consuming and becomes unsuitable for optimization, which needs to repeat many times.

To understand the conventional method to simulate the ISF function, Fig. 2.11 can be utilized.

Power Reduction with Phase Noise Improvement

Several low-power LC-VCO candidates are shown in Fig. 2.12. To lower the power consumption, the conventional CMOS-type VCO is a strong candidate with lower power consumption and sufficient phase noise performance. However, when the current is limited to lower than 200 µA, we notice that introducing the PMOS transistor in the low-power design is inappropriate because of the much large transistor size (compared with NMOS transistor). To maximum g_m at the start-up condition, the center bias should be fixed to VDD/2 to make both the PMOS coupled pair and the NMOS coupled pair work in the saturated region. Thus, the size of the PMOS transistor has to be double (typically, the

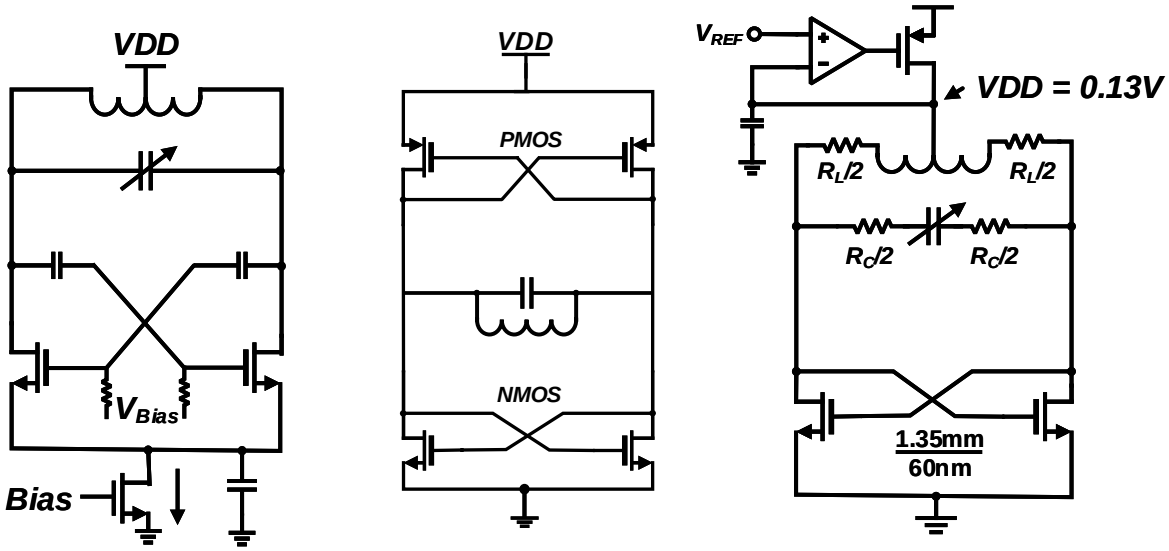


Figure 2.12: Candidates for the low-power LC-VCO design.

ratio of the PMOS and the NMOS transistor are equal to 2). Since the transistor has to be enlarged to maximum the g_m with the limited power. The introduced PMOS transistor will introduce a much large low-Q capacitance, which degrades the total quality factor of the bank. Also, due to the non-linear gate capacitance, the noise up-conversion occurs through this non-linear capacitance. The maximum available oscillation frequency is also limited due to the large parasitic capacitance.

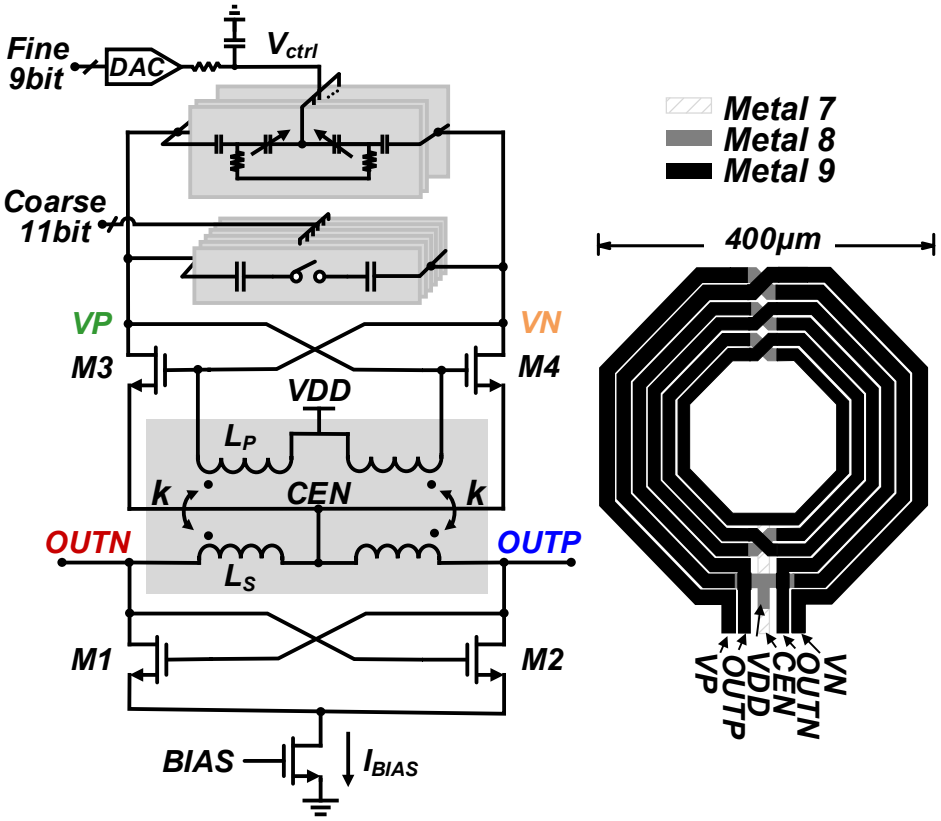
Here, we discuss a little about the class-D structure, which benefits from its low-voltage operation. By lowering the power supply, the class-D type VCO seems can be a candidate as a low-power design. However, in the actual case, the current of the class-D type transistor can't be limited due to the lack of a current source. Also, to realize the switch function, a large size of transistor (> 1 mm) should be implemented, which leads to a huge current pulse in each period. Meanwhile, the huge transistor size inevitably introduces a large non-linear and low-Q capacitance. This capacitance limit the maximum available oscillation frequency and lower the total quality factor of the bank (degrade the phase noise performance), while serious noise up-conversion occurs through non-linear capacitance. That is why the measured flicker corner of the class-D type VCO is around 1 MHz [20] while a conventional Class-B type VCO can achieve 200~300 kHz flicker corner performance.

2.2 Proposed Gm-Stacked VCO using Transformer

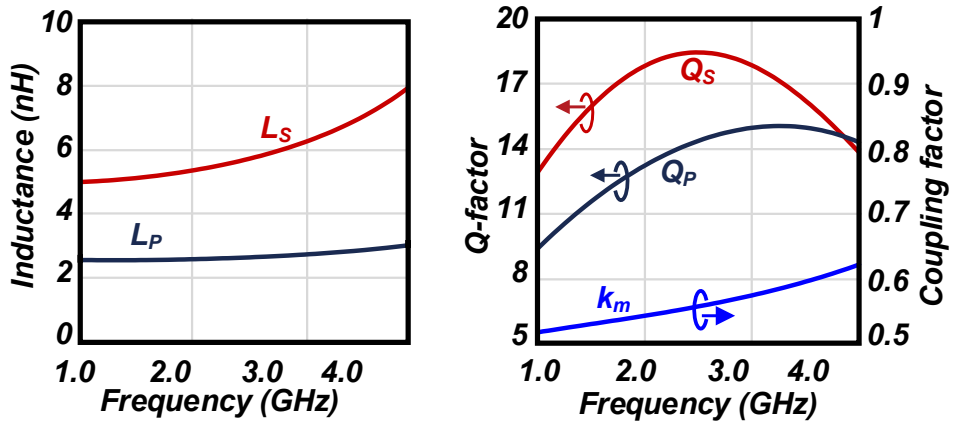
To lower the power consumption of the oscillator in a PLL, a ring oscillator can be utilized [21]. However, a ring oscillator has poor phase noise comparing with the oscillator, which significantly degrades PLL phase noise. LC oscillators are still the solution to improve the PLL noise performance due to the high quality factor (Q-factor) of the frequency selectivity provided by the LC resonator. The conventional CMOS-type LC DCO [15, 22] is advantageous for obtaining a larger output swing in the current-limited region, in which the output swing V_{AMP} is mainly limited by the available tank impedance. Hence, it is inevitable that for achieving low current consumption, large size cross-coupled pairs are required. However, the introduced parasitic capacitance from the large NMOS and PMOS transistors limits the load inductance and degrades the Q-factor of the tank. Thus, utilizing conventional CMOS-type DCO in a DPLL targeting for lower than 300-μW power consumption becomes extremely difficult. Some transformer-based DCOs with current-reuse structure have been proposed to lower their power consumption [23][24][25].

The proposed TF-based DCO [26] is developed to have sufficient output amplitude with minimum power consumption. A transformer-based resonator is treated as a two-port network to build the oscillator. Both of the top and bottom cross-coupled pair use the NMOS transistors to provide the negative resistances to attain a large Gm from each transistor, as shown in Fig. 2.13(a). The stacked cross-coupled pairs share the same DC current. The center tap of the primary winding is connected to a voltage source while the DC current flows into the bottom cross-coupled pair through the center tap of the secondary winding. The coupling of the transformer corresponds to positive feedback between the top and bottom oscillators. The transistor sizes in the top cross-coupled pair are 128 μm/60 nm, and the gate length is 256 μm for the bottom cross-coupled NMOS pair. Using the NMOS transistors instead of PMOS relaxes the current requirement, which benefits from its higher mobility. Compared with low-power class-D VCOs shown in [20][27], a relatively small transistor size is implemented. Therefore, a higher oscillating frequency and a wider frequency-tuning range can be achieved.

A higher Q-factor of the load inductance is desired in both of the windings to provide sufficient load impedance for both cross-coupled pairs. To mitigate the Q-factor degradation, a 2:4 co-planar TF structure is adopted, while only one cross-section exists in the TF to connect with the power supply, as shown in Fig. 2.13(a). In the EM simulation shown in Fig. 2.13(b), the inductance of the primary winding (L_P) and secondary winding (L_S) are 2.7 nH and 6.0 nH at 2.4 GHz, respectively. The magnetic coupling coefficient (k_m) is 0.56, while the Q-factor of the primary winding (Q_P) and secondary winding (Q_S) achieve 14.4 and 18.3, respectively. A frequency tuning range from 2.1 GHz to 3.1 GHz

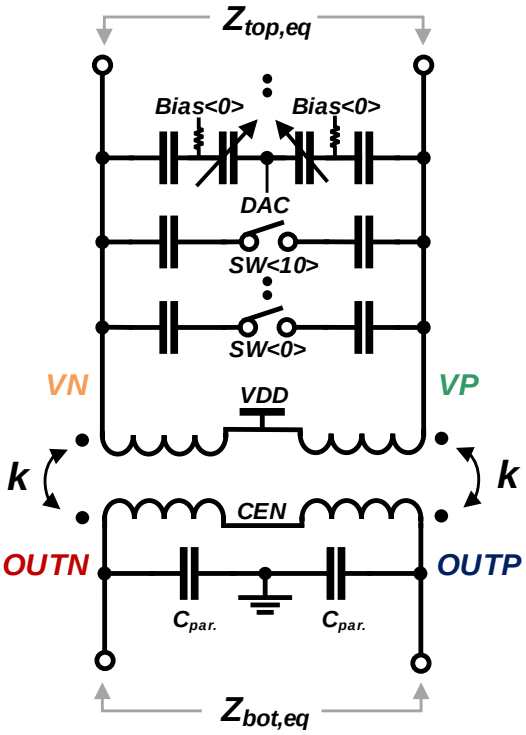


(a)

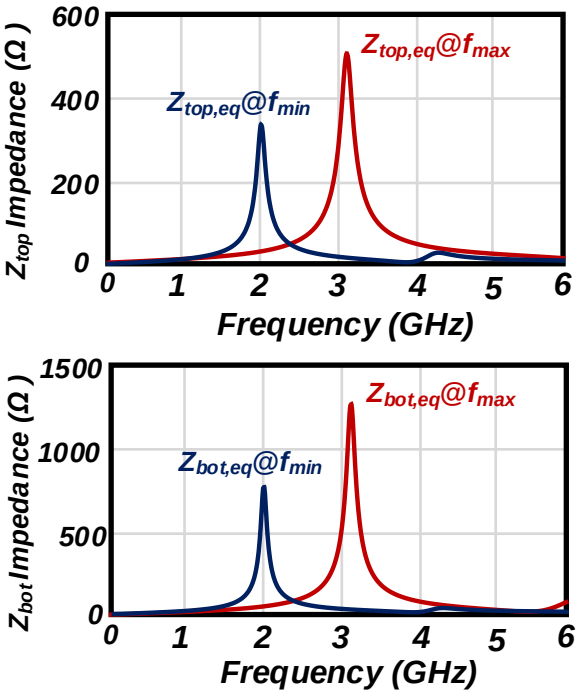


(b)

Figure 2.13: (a) Proposed transformer-based stacked-gm DCO (b) Transformer with EM simulation results.



(a)



(b)

Figure 2.14: (a) Transformer with capacitor banks (b) Simulated input impedance from the top side and bot side.

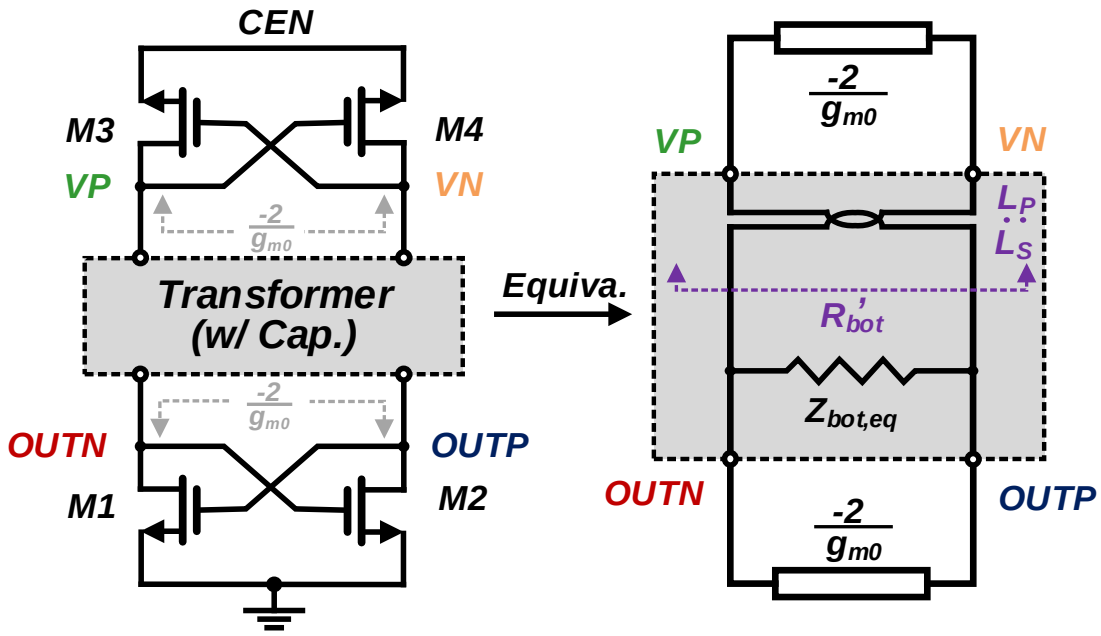


Figure 2.15: Schematic redrawn of the proposed DCO and equivalent circuit.

is available from the cooperation of the primary winding, which has a relatively smaller inductance, and an 11-bit coarse capacitor bank. The large inductance L_S ensures the start-up with a small current. The positive feedback between the coupled windings provides sufficient output amplitude for the DPLL feedback.

Fig. 2.14(a) provides the details of the tanks, a linearized varactor bank is implemented for the fine-frequency tuning, and the switch-controlled-capacitor bank is used for the coarse-frequency tuning. As derived in [28], the main resonant frequency ω_L of the tank can be estimated as

$$\omega_L^2 = \frac{1}{L_P C_P (1 + |k_m|)} \tag{2.19}$$

The C_P and C_S represent the top and bottom capacitance. As discussed in [28][29][30], there is another possible resonant frequency ω_H. To avoid the multi-oscillation behavior in the DCO operation, the capacitor ratio of C_P and C_S is designed to ensure $L_S C_S / L_P C_P$ in the range of $1.1 \sim 2.59$, at $2.1\,\text{GHz} \sim 3.1\,\text{GHz}$. Thus, only a small equivalent tank resistance exists at ω_H [29]. Note that in the ULP DCO design, the transconductance gain is also too small to maintain the oscillation with the low resistance.

The input impedance of the tank Z_{in} has been discussed in [28]. The $Z_{top,eq}$ and $Z_{bot,eq}$ are the differential input impedances from each side of the transformer (primary and secondary) without loading [28], and the simulated results are shown in Fig. 2.14(b).

Thanks to the transformer with large inductance and relatively high Q-factor, a 320 Ω $Z_{top,eq}$, and a 750 Ω $Z_{bot,eq}$ are available at lower frequency boundary.

As shown in Fig. 2.15, the cross-coupled transistors must provide sufficient transconductance (g_m) to start the oscillation in the transformer. To obtain the minimum required g_m, the parallel resonance model in [28] is applied in the equivalent circuit. The load impedance of M1 and M2 transistor is equivalent to the parallel combination of $Z_{bot.eq}$ and the transformed load impedance R'_{bot}. In case of all the transistors (M1∼M4) have the same g_{m0}, the negative resistance can be obtained as $-2/g_{m0}$. According to the designed value of $L_S C_S / L_P C_P$, the load impedance transfer ratio can be expressed as the turn ratio $L_P : L_S$ [28]. Meanwhile, R'_{bot} can be recast as $L_S/(-g_{m,M4}L_P)$ and $Z_{bot,eq} = \omega_L L_S Q_S (1+k)^2/(1+Q_S/Q_P) \approx \omega_L L_S Q_S$. Thus, the start-up condition is given as:

$$g_{m0} > \frac{2}{(1+\frac{L_P}{L_S})\omega_L L_S Q_S} \tag{2.20}$$

Note that both of the top and bottom cross-coupled pairs implements the NMOS transistor as the active devices, which can provide higher g_{m0} compared with the same size of PMOS transistors.

To reduce the total power consumption of the PLL feedback path, the oscillator's output amplitude should be high enough so that the buffers' power demand can be alleviated. In a conventional CMOS type oscillator, the output amplitude can be expressed by using $4I_{BIAS}\omega LQ/\pi$. An inductor with a large inductance L can improve the output amplitude, but the lower Q-factor and self-resonate frequency will limit its application in the ULP oscillator designs. In the transformer-based DCO, the transformer based resonator can offer the voltage gain above $k_m N$, as demonstrated in [29]. According to the value of $L_S C_S / L_P C_P$, the input impedance of the tank $Z_{top,eq}$ can be simplified [28] as:

$$Z_{top,eq} = \omega_L L_P Q_P \frac{(1+k_m)^2}{1+Q_P/Q_S} \tag{2.21}$$

The output amplitude at the OUTN/OUTP node can be estimated as

$$V_{AMP} \approx \frac{4}{\pi} I_{BIAS} \frac{Z_{top,\omega_L}}{2} k_m N + \frac{4}{\pi} I_{BIAS} \omega_L \frac{L_S}{2} Q_S \tag{2.22}$$

The $Z_{bot,eq}$ is estimated as $\omega_L L_S Q_S$ depending on the value of $L_S C_S / L_P C_P$ from 1.1 to 2.59 across the frequency tuning range [28]. In the case of the $k_m = 0.56$, the V_{AMP} can be simplified using the mentioned parameters. (L_P = 2.7 nH and L_S = 6.0 nH corresponding

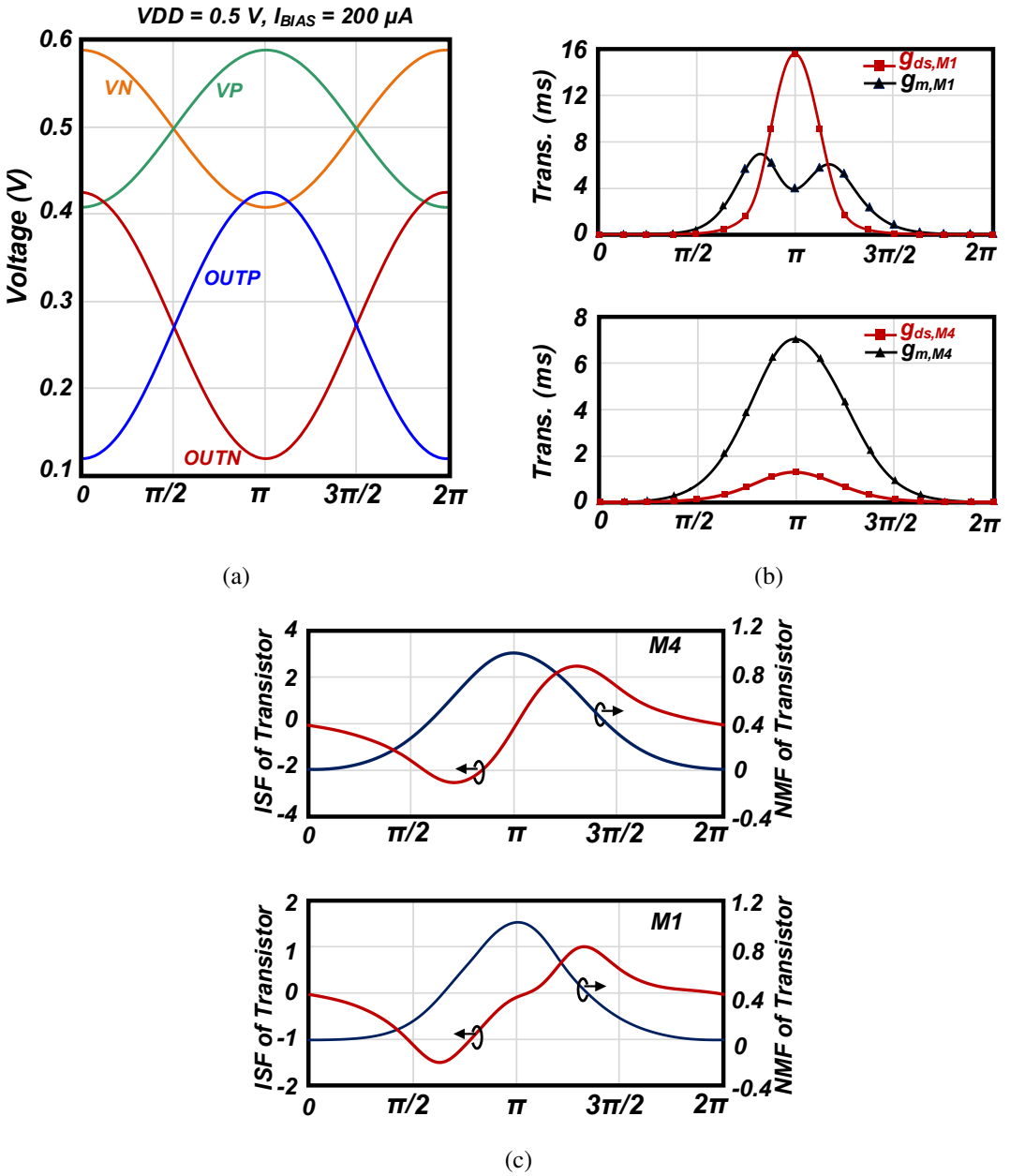


Figure 2.16: (a) Simulated transient voltage waveforms of both cross-coupled pair (b) Simulated transconductance and channel conductance of M1 and M4 transistors (c) Simulated ISF and NMF of the M1 and M4 transistors in the proposed DCO.

	Proposed (This work)	CMOS	NMOS
Current	I_{BIAS}	I_{BIAS}	I_{BIAS}
Parasitic Capacitance.	NMOS x 4	NMOS x 2 + PMOS x 2	NMOS x 2
Start-up Gm (Minimum)	$g_{m0} > \frac{2}{(1+L_P/L_S)\omega_L L_S Q_S}$	$g_{m0} > \frac{1}{\omega L Q}$	$g_{m0} > \frac{2}{\omega L Q}$
Output Amplitude	$\approx \frac{4}{\pi} I_{BIAS}\, \omega_L \frac{L_P}{2} Q_P \frac{1}{(k_m^2 N + k_m N + \frac{L_S Q_S}{L_P Q_P})}$	$\frac{4}{\pi} I_{BIAS}\, \omega L Q$	$\frac{2}{\pi} I_{BIAS}\, \omega L Q$
Area	Transformer x 1	Inductor x 1	Inductor x 1

Figure 2.17: Theoretical comparison between the proposed TF-based structure and conventional structures.

to Q_P = 14.4 and Q_S = 18.3).

$$V_{AMP} \approx \frac{4}{\pi} I_{BIAS}\, \omega_L \frac{L_P}{2} Q_P (k_m^2 N + k_m N + \frac{L_S Q_S}{L_P Q_P}) \tag{2.23}$$

Fig. 2.16(a) shows the simulated transient waveform. With a 200 µA DC current, a 300 mV V_{AMP} can be obtained in the post-layout simulation. The output amplitude is a linear relation with a bias current of lower than 250 µA current, and the proposed DCO starts entering the voltage limited region with a larger current.

The proposed TF-based stacked-gm DCO guarantees oscillation at all the PVT corners with 200 µA current consumption. Fig. 2.16(b) shows the simulated transconductance and channel conductance of the active devices. The simulated NMF and effective ISF of the M1 and the NMF of the M4 transistors are shown in Fig. 2.16(c). Compared to the conventional class-B type DCO, the effective noise power of the active devices is close to the conventional designs. The simulated phase noise is -107dBc/Hz at 1MHz at a very low power consumption of 100 µW. The phase noise contribution is mainly from the tail transistor, which can be improved by replacing it with a tunable resistor or the tail inductor. An inverter-based with resistor feedback DCO buffer is adopted to minimize its power consumption. With a 300 mV output swing from the DCO, the buffer and the sampler only consumes 54 µW in post-layout simulation. Theoretical comparison between the proposed TF-based structure and conventional structures is shown in Fig. 2.17. Benefits from the passive gain in the transformer, the required minimum start-up gm is reduced while the output amplitude is enhanced.

Compared with the conventional CMOS structure VCO design, avoiding PMOS tran-

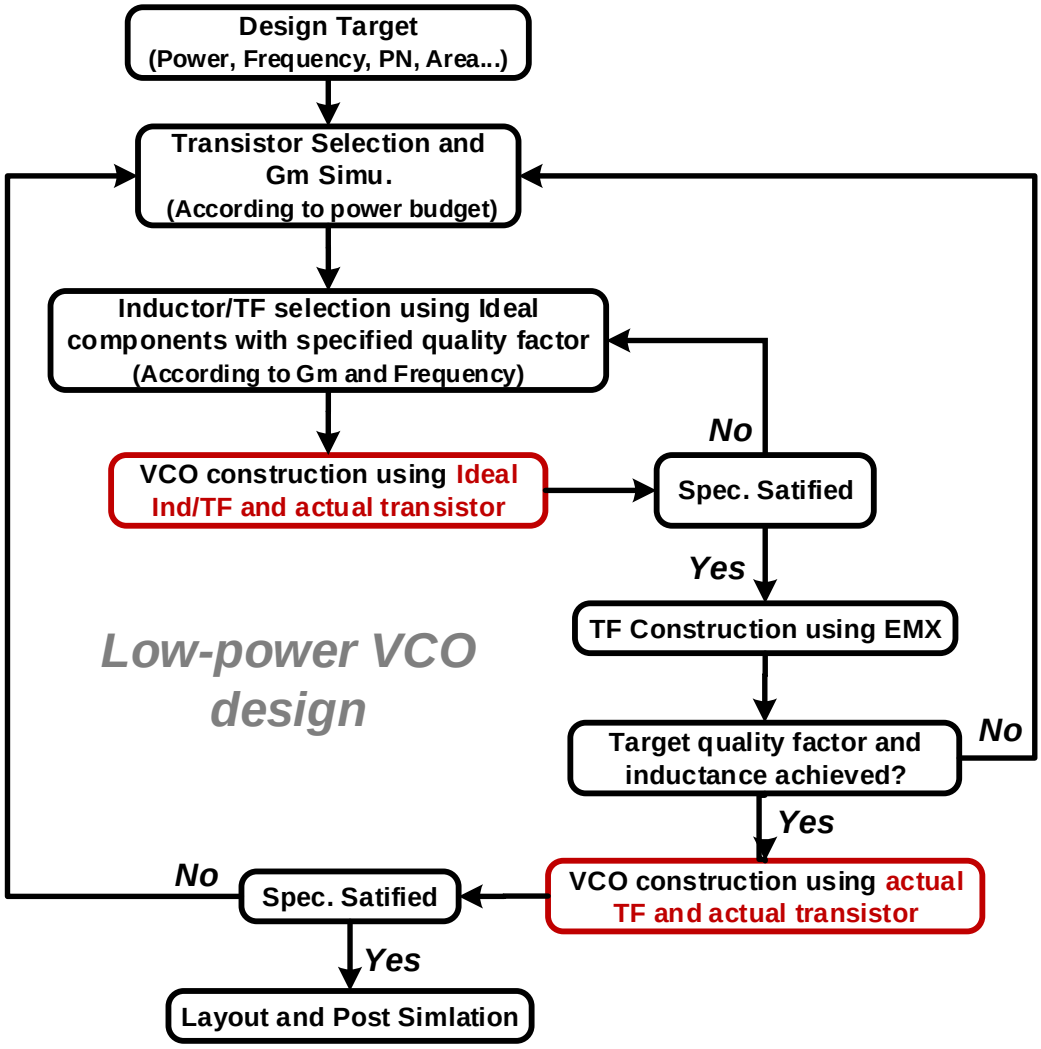


Figure 2.18: Design procedures of transformer-based VCO.

sistor implementation can obtain the same transconductance while introducing smaller parasitic capacitance. That improves the oscillation frequency and relaxes the inductance selection. The theoretical start-up Gm calculation indicates that the Gm also benefits from its passive gain between primary and secondary windings. The theoretical amplitude calculation of the steady-state of the oscillation proves the characteristics of the transformer highly determine the output amplitude. Thus, a higher coupling factor and passive gain are desired.

2.3 Design Procedures of Transformer-Based VCO

Fig. 2.18 shows the general design procedures of the transformer-based VCO. Typically, the first step of the VCO design is choosing a proper transistor. What should be noticed

here is that the transistor selection method for better phase noise performance and lower power performance is totally different. The detailed optimization of the conventional LC-VCO can be found in [31]. According to the power budget, the transistor size must be specified. In this step, two points must be considered. One is the introduced parasitic capacitance, which will limit the inductance value and oscillation frequency, and another one is the minimum Gm for robust start-up must higher than the theoretically calculated value (*e.g.,* two times). The usage of ideal component (*e.g.,* MIND and INDQ components in Cadence analoglib) can simplify the transformer design with specified values. What should be noticed is that the specified should close to the real cases (need several tests and on-chip inductor/transformer design experiences). If the simulation results can be achieved with the specified value, then go to the next step with building the actual transformer and use this transformer in a real VCO design. As shown in the design flow, there are feedback loops. In case of the goal cannot be met, we need to reconsider the design goals.

2.4 Area-Reduction and Supply Pushing Reduction

The PN performance of LC-VCO is highly determined by the load tank's quality factor (Q) [32]. Thus, to reduce the total on-chip area, the area of the inductor can be minimized while ensuring a specific Q value and inductance. To reduce the losses introduced by the low-resistance silicon substrate, the PGS is employed as a terminal to the electric field leaking into the substrate [33]. The abundant silicon under the PGS can potentially be used for the other components, as shown in Fig. 2.19. With assistant from the PGS, the circuitry associated with the VCO can be placed underneath the inductor or transformer built by using ultra-thick metal (UTM) layer. Thus, the on-chip area can be further shrunk.

Conventional complementary LC-VCO has been introduced from the last century to reduce power consumption [34] and has been improved with a lower power consumption [35]. As we noticed, it is inappropriate to introduce the large PMOS transistors in a ULP VCO design (*e.g.,* $\leq 120\,\mu W$). To maintain a constant oscillation with a small current, the VCO transistors have to be large enough to provide sufficient transconductance. However, the parasitic capacitance of the PMOS transistor heavily degrades the Q-factor of the total tank, and it will also limit the available inductance and oscillation frequency. To mitigate the usage of the PMOS transistor and maintain an adequate PN performance with about $100\,\mu W$ power consumption, a current-reused TF-based LC-VCO, which uses NMOS only as the negative resistance is introduced. The transformer is designed to have large inductance for both primary and secondary windings with a compact on-chip area.

Those portable devices powered by the batteries use dc-dc converters to transform the

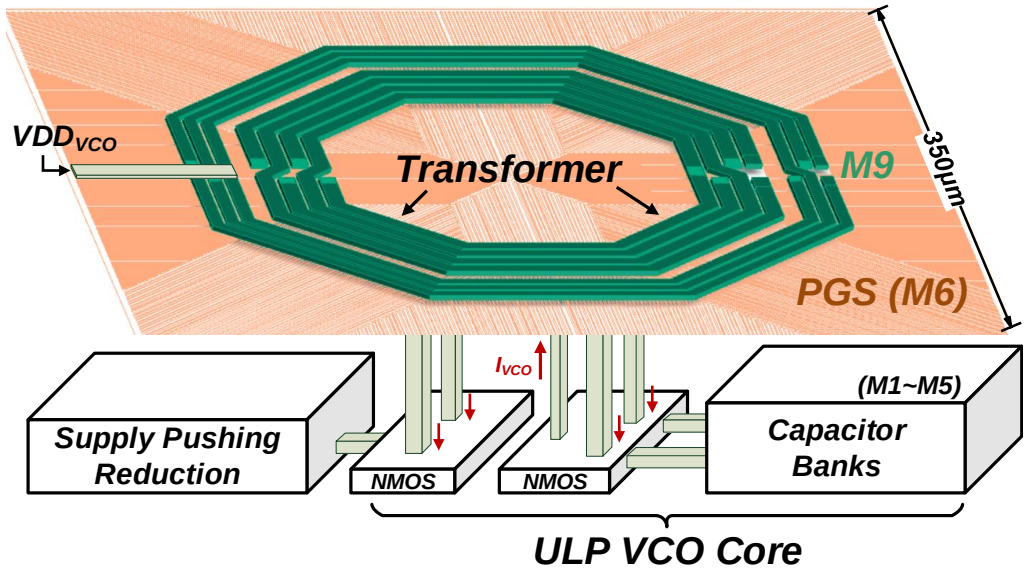


Figure 2.19: ULP transformer-based VCO with minimized on-chip area and supply pushing reduction.

voltage of power sources to the acceptable voltage level of the circuitry. Thus, the output voltage ripples inevitably exist in the output node. Meanwhile, the VCO frequency is heavily influenced by the unstable voltage supply. Large spur will present in the output spectrum, which degrades the PLL performance heavily and the TRX performance. Thus, a conventional off/on LDO is generally implemented to suppress those voltage ripples and drops. However, an additional voltage headroom is required for the LDO implementation, which also means the voltage efficiency is directly decreased. To avoid the additional voltage headroom requirement and improve the total power efficiency, a low-power and block-simplified supply pushing reduction loop is proposed by directly controlling one of the cross-coupled transistor bias points.

This chapter presents a miniaturized transformer-based ultra-low-power (ULP) LC-VCO with embedded supply pushing reduction techniques for IoT applications in the 65-nm CMOS process. To reduce the on-chip area, a compact transformer patterned ground shield (PGS) is implemented. The transistors with switchable capacitor banks and associated components are placed underneath the transformer, which further shrinking the on-chip area. To lower the power consumption of VCO, a gm-stacked LC-VCO using the transformer embedded with PGS is proposed. The transformer is designed to provide large inductance to obtain a robust start-up within limited power consumption. Avoiding implementing an off/on-chip Low-dropout regulator (LDO), which requires additional voltage headroom, a low-power supply pushing reduction feedback loop is integrated to mitigate the current variation. Thus the oscillation amplitude and frequency can be

stabilized. The proposed ULP TF-based LC-VCO achieves phase noise of -114.8 dBc/Hz at 1 MHz frequency offset and 16 kHz flicker corner with a 103 µW power consumption at 2.6 GHz oscillation frequency, which corresponds to a -193 dBc/Hz VCO figure-of-merit (FoM) and only occupies 0.12 mm^2 on-chip area. The supply pushing is reduced to 2 MHz/V resulting in a -50 dBc spur, while 5 MHz sinusoidal ripples with 50 mV_{PP} are added to the DC supply.

2.4.1 Transformer with Patterned Ground Shields

As an essential part of PLL, as mentioned earlier, VCOs are desired with sufficient PN performance and power consumption as low as possible. As one of the state-of-the-art PLL shows [15], the VCO takes more than 40% of the total power consumption. Some Low-power VCOs have been introduced with significant power reduction [35–39]. However, several of them achieve sufficient PN (*e.g.,* ≤ -110 dBc/Hz at 1-MHz frequency offset in BLE TRX), low-power (≤ 120 µW), and small on-chip area (≤ 0.15 mm^2) simultaneously. Thus, a low-power and compact LC-VCO is suitable for long-lifetime and low-cost IoT applications. In this section, the operation of the proposed TF-based compact and low-power VCO will be elaborated.

In low output power BLE TRX designs [14][15], the PLL can consume more than 30% of the TX total power. However, according to the BLE standard, a ± 50 kHz frequency shift can be tolerated within a single packet, which indicates that the TX can modulate the VCO frequency directly using an open-loop operation after the PLL is turned off. Consequently, higher TX efficiency can be achieved [17]. The latest VCO frequency shift is from the oscillator's residual FM noise and also the variation from the DC supply and temperature. To realize a maximum ± 50 kHz frequency shift with consideration for voltage and temperature variation, the residual FM (Δf_{FM}) should be less than 2.4 kHz with a 20% margin, according to [17]. The Δf_{FM} of VCO's can be calculated by

$$\Delta f_{\mathrm{FM}} = \sqrt{2 \int_{f_{\mathrm{a}}}^{f_{\mathrm{b}}} (\Delta f) \cdot \mathscr{L}(\Delta f) \cdot d(\Delta f)} \tag{2.24}$$

in which $\mathscr{L}(\Delta f)$ represents the VCO phase noise at the offset frequency Δf, and according to [17], the integration range is from 50 Hz (f_{a}) to 1 MHz (f_{b}), which is determined by the packet length and the FSK symbol rate respectively. A VCO with good $1/f^2$ PN performance is a potential candidate for the open-loop operation, even with a moderate flicker noise performance. However, to achieve a good $1/f^2$ PN, larger power consumption with a higher Q-factor is required at the same time according to Leeson's equation, and that conflicts with the low-power and compact area demanded by the IoT applications.

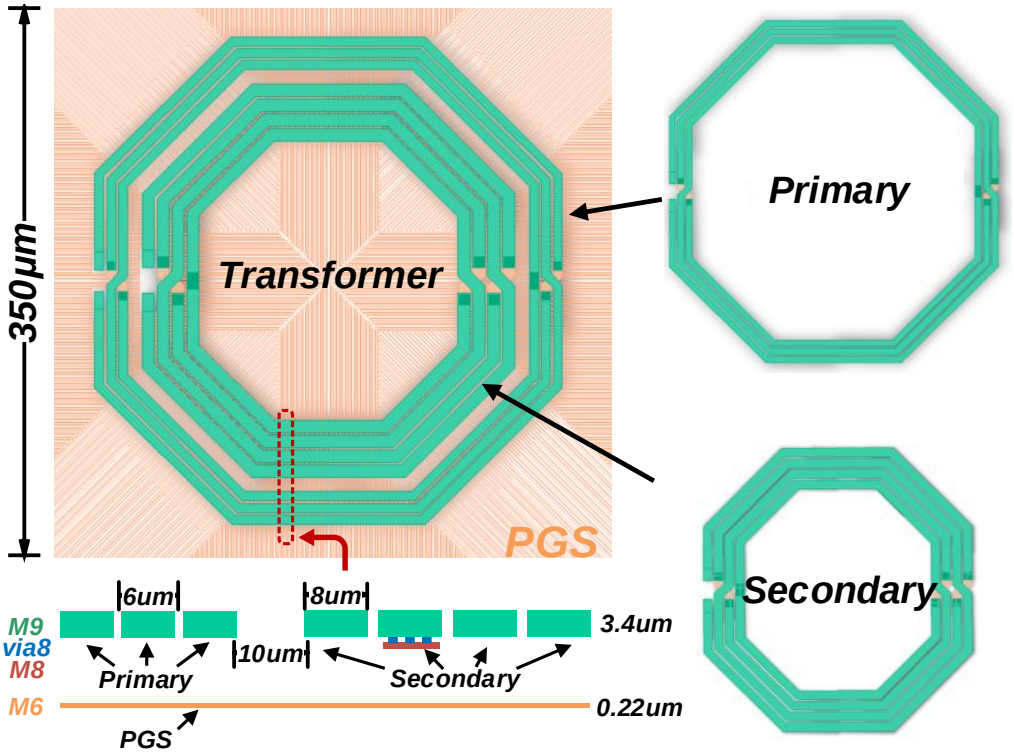


Figure 2.20: Transformer with PGS.

As a result, a low-flicker noise VCO with sufficient $1/f^2$ PN performance is much more appreciated for TRX implemented in IoT applications. Oscillator phase noise has been discussed and analyzed in [40][41][42]. As demonstrated in equation (51) in [42], the up-converted flicker noise in a conventional CMOS-type VCO can be estimated as single sideband to carrier ratio (SSCR) at frequency ω_m as

$$SSCR_{\omega_m} = \left(\frac{K_F^n}{C'_{ox}L_n^2} + \frac{K_F^p}{C'_{ox}L_p^2}\right)\left(\frac{2\pi}{\omega_m^3}\right)\cdot\frac{(G_X^2-1)^2\omega_0}{2\cdot 32^2 A_1 Q^3 C} \tag{2.25}$$

where $K_F^{n,p}$ and C'_{ox} are process dependent constants, $L_{n,p}$ is the MOS channel length, A_1 the amplitude of fundamental frequency, Q the quality factor of the tank, ω_0 the oscillation frequency. A lower flicker noise corner can be achieved by appropriately selecting the excess gain, which is defined as $G_X = g_m \cdot R$ where g_m is the small-signal transconductance of the cross-coupled transconductance and R is the tank impedance, or improving the Q factor of the tank. In this work, both of the transistor size and the transformer shape are optimized to achieve a minimum $G_X \approx 2$ with a lower than 100 μW power. Equation (2.25) also indicates that a large fundamental amplitude A_1 also helps reduce the flicker noise.

To achieve a VCO with low-power consumption and good PN performance, the in-

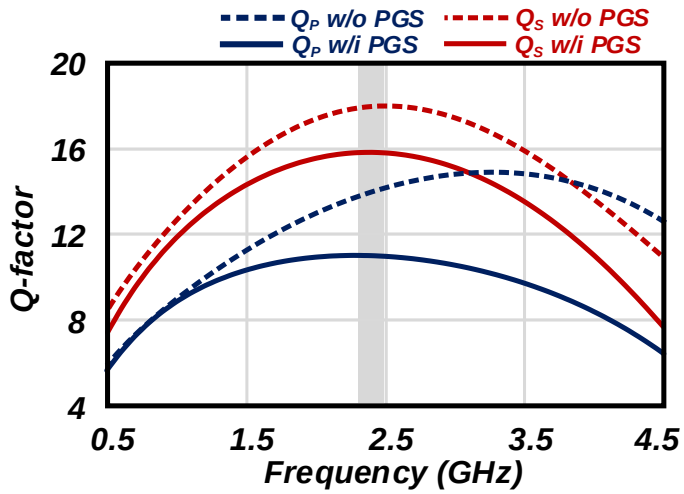


Figure 2.21: EM simulation results of the transformer with and without the PGS

ductor/transformer is the critical component that is needed to provide a large inductance with a high enough Q-factor. Generally, the total tank's Q-factor and available impedance are primarily dependent on the inductor/transformer's performances. Because of its importance, the inductor/transformer needs to be carefully designed and modified.

Fig. 2.20 shows that the transformer includes a PGS, which is built with the intermediate layer (M6). Usually, only one UTM layer exists in modern CMOS technology. In this implemented 65-nm process, the top metal (M9) is the thickest metal, which is 3.4 µm and beneficial to build a high Q-factor inductor/transformer. The co-planar TF structure can be potentially more area-efficient [43]. However, due to the lack of multi-layer thick metal, the Q-factor will be degraded due to the multiple crossing intersections, which is inevitable in TF with a large inductance value. Both the primary and secondary windings are symmetrical and embedded with center taps. To maximize the inductance of both windings, the primary is constructed with three turns, and the secondary winding has four turns. Due to the large capacitance between the windings and the PGS layer, the width of windings has to be chosen with sufficient self-resonating frequency. To realize a VCO oscillating at 2.4 GHz, the self-resonating frequency is designed to be more than 5 GHz. Fig. 2.21 and Fig. 2.22 show the electromagnetic (EM) simulation results.

The inductance of primary and secondary windings are 3.2 nH (L_P) and 6.7 nH (L_S), respectively, which is shown in Fig. 2.22. The Q-factor of the first winding (Q_P) exceeds 10, and the Q-factor of the secondary windings (Q_S) achieves 16, as shown in Fig. 2.21. A comparison of the Q-factor between with and without PGS is also observed through Fig. 2.21. Due to the large capacitance between the windings and the PGS, the self-resonating frequency is decreased from more than 7 GHz to 5.5 GHz. Though the co-planar TF structure is utilized with separated windings, both windings show strong

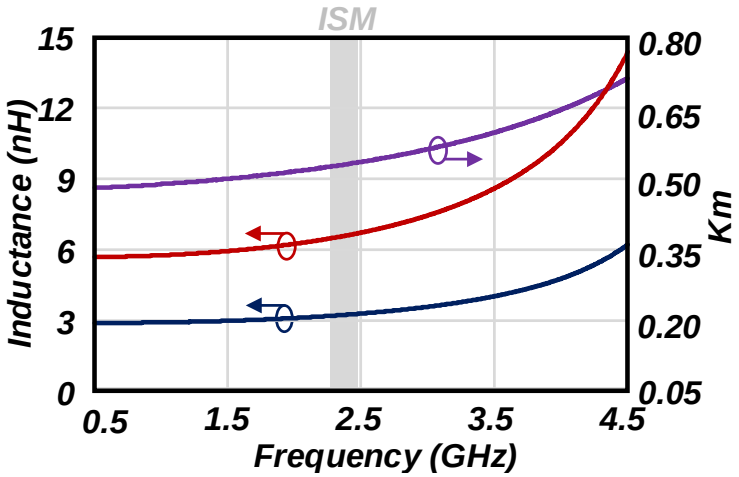


Figure 2.22: EM simulation results of the transformer: inductance and coupling factor.

coupling, and the coupling factor (k_m) is over 0.5. Thanks to the large inductance from the secondary windings with high Q-factor, the large enough resonant impedance is available from the secondary winding, and thus a robust start-up with an ultra-low current consumption can be realized.

There are 10 µm spacing between the primary and secondary windings. By changing this spacing, the mutual inductance (coupling factor) can be controlled. The simulated coupling factor, quality factor, and inductance of secondary winding are shown in Fig. 2.23(a) and Fig. 2.23(b). Notice that the outer radius is kept constant. To avoid the multiple oscillation frequency [29], a large than 0.5 coupling factor is realized with 10 µm spacing. Also, the quality factor is nearly constant with larger spacing, but the inductance is decreased as linear. A 10 µm spacing also can realize both large inductance and the high-quality factor for the secondary winding.

With the implementation of the PGS, 20% area reduction can be realized in this VCO with only slight PN degradation ($<$1 dB in simulation) due to the minimal Q-factor degradation ($<$2). A higher area efficiency can be realized when this TF-based VCO is implemented in the TRX design because the large digital components and analog circuitry constructed using low-level metal can be placed underneath the TF together.

Note that this PGS technique presented here is only implemented in this VCO design and not implemented in BLE transceiver design, which will be introduced in next Section 3. As indicated in Fig. 2.21, the quality factor is heavily decreased due to the implementation of the PGS, while the quality factor will determine the power transfer efficiency [44]. That is the main reason why there is no PGS for the transformer in the BLE transceiver design. Since the active transistor is put underneath the PGS, the influence between the transformer and the transistor should also be considered. According to the

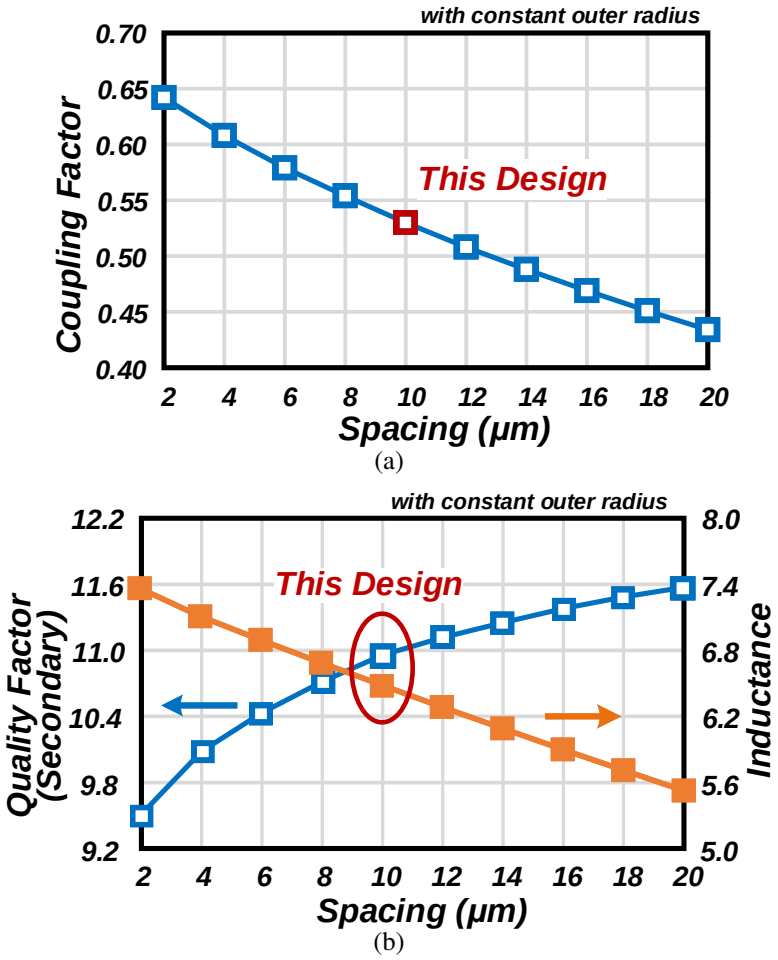


Figure 2.23: EM simulation results with tuning the spacing between primary and secondary windings.

Table 2.1: VCO SIMULATION RESULTS WITH AND WITHOUT THE PGS (SAME CURRENT BIAS CONDITION).

	w/ PGS (Sim.)	w/o PGS (Sim.)
Architecture	TF	TF
Tech. (nm)	65	65
Freq. Range (GHz)	2.52∼2.77	2.96∼3.21
Center Freq. (GHz)	2.645	3.09
DC Supply (V)	0.5	0.5
Osc. Power (μW)	103	103
PN@ 1MHz (dBc/Hz)	-115.1	-114.3
Area (mm^2)	0.12	0.17

author's understanding, the PGS has a negligible direct impact on the transistor, which only introduces a little bit of parasitic capacitance. But it can reduce coupling between the transformer with bottom wire traces.

Table 2.1 shows the simulation results with and without the PGS. Since the PGS introduces large parasitic between the transformer and ground, the center frequency decrease around 440 MHz. The quality factor also influences the phase noise performance of the VCO design. The area estimation without the PGS will be much larger than with the PGS case. Table 2.2 shows the comparison of the results between the measurement and EMX simulation results (with PGS). There are two reasons for the additional frequency degradation. The first one is the PGS has introduced more parasitic capacitance because the active transistor has to be removed in EMX simulation. Also, the process and temperature variation have a large influence on the oscillation frequency. Typically, the inductance variation is relatively small $\leq \pm 5\,\%$. Meanwhile, the maximum possible capacitance variation is around 20 %. Also, because all the tested chips are from the same die, it is possible that the process corner heavily influences center frequency.

2.4.2 Supply Pushing Reduction

Conventional CMOS-type LC-VCO has been widely utilized in low-power PLL and TRX designs [11, 14, 15], which is advantageous for obtaining a large output amplitude while working in the current-limited region, as shown in Fig. 2.24. However, to further reduce the power consumption of the CMOS-type LC-VCO and maintain a good PN is somehow tricky [15]. In an ultra-low-power LC-VCO design, *e.g.,* $\leq 120\,\mu$W, the transistors have to be large enough to increase current efficiency or obtain a larger g_m with the same current consumption. However, what should be noticed is that the PMOS transistors introduce

Table 2.2: VCO PERFORMANCES COMPARISON BETWEEN EMX RESULTS AND MEASUREMENT (SAME CURRENT BIAS CONDITION).

	Measurement	EMX (w/ PGS)
Architecture	TF	TF
Tech. (nm)	65	65
Freq. Range (GHz)	2.39∼2.64	2.52∼2.77
Center Freq. (GHz)	2.515	2.645
DC Supply (V)	0.5	0.5
Osc. Power (μW)	103	103
PN@ 1MHz (dBc/Hz)	-114.8	-115.1
Area (mm^2)	0.12	0.12

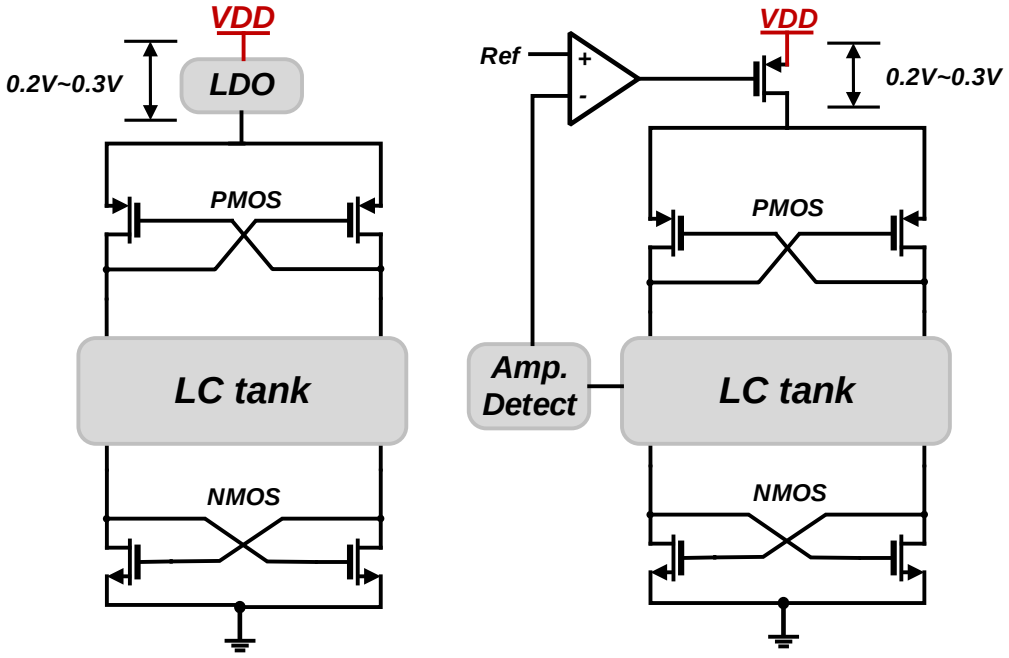


Figure 2.24: Conventional CMOS structure with supply pushing reduction technique of typical LDO implementation and amplitude tracking feedback.

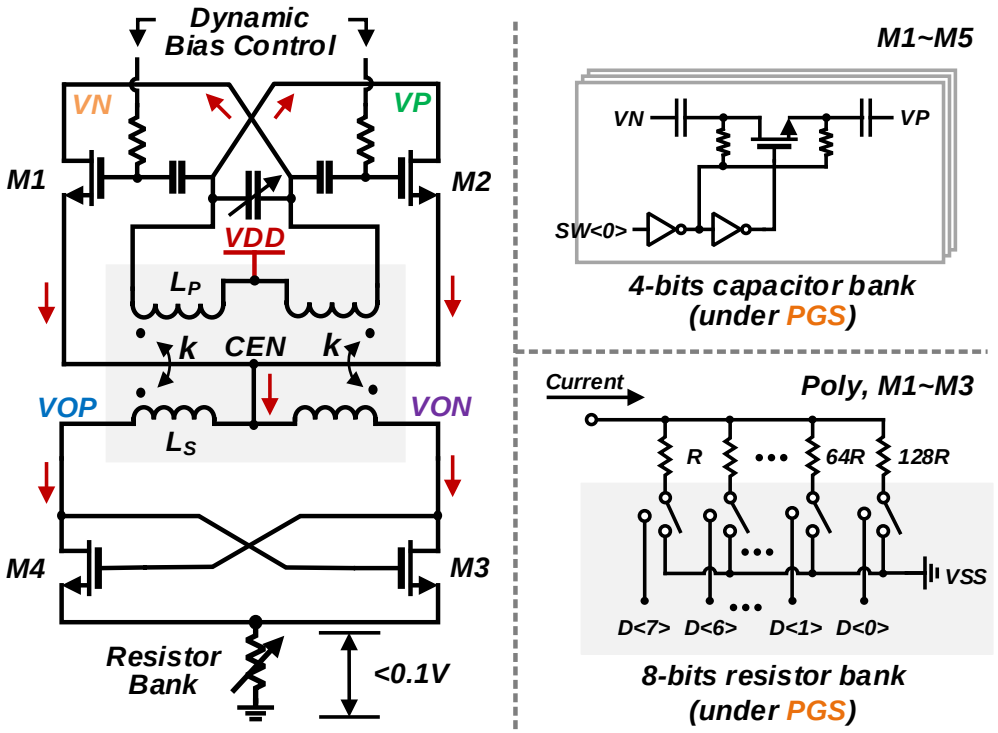


Figure 2.25: TF-based LC-VCO with 4-bits capacitor banks and 8-bits resistor banks.

large low-Q parasitic capacitance. The low-Q parasitic capacitance will heavily decrease the Q-factor of total banks, consequently, limit the available tank impedance and oscillation frequency. Also, due to the non-linear characteristic of the parasitic capacitance, the up-converted flicker noise will increase from the larger harmonic distortion, and the $1/f^2$ PN will also be degraded due to the lower-Q factor. The NMOS transistor has higher mobility compared with the PMOS transistor with the same size. A lower DC voltage implementation is also helpful in reducing power consumption with a slightly larger current. The class-D VCO, which can operate with an ultra-low VDD (*e.g.,* 0.2 V), is a potential candidate for the low-power design. However, the low-voltage operation requires an additional LDO, which degrades the voltage efficiency. The huge supply pushing makes the LDO more important [38].

The proposed TF-based DCO is developed to have sufficient output amplitude with minimum power consumption. A TF-based resonator is treated as a two-port network to build an oscillator [45] with the double cross-coupled NMOS transistors providing negative g_{m}. Both of the top and bottom cross-coupled pair use the NMOS transistors to provide the negative resistances to attain a large Gm from each transistor, as shown in Fig. 2.13(a). The same DC current is shared by the stacked cross-coupled pairs. The center tap of the primary winding is connected to a voltage source while the DC current flows into the bottom cross-coupled pair through the center tap of the secondary winding. The

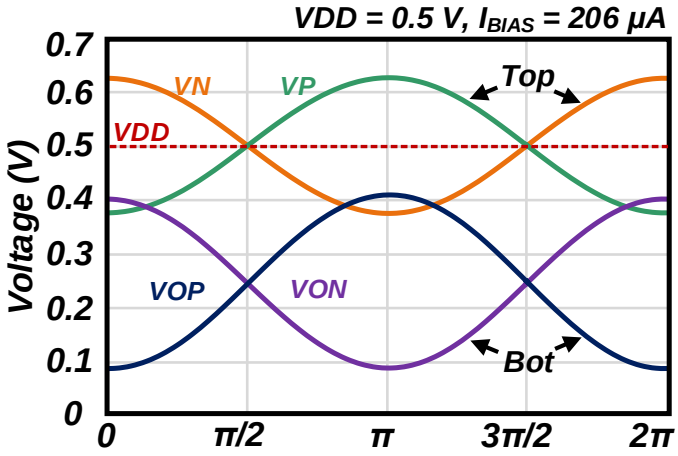


Figure 2.26: Simulated waveform of each point in the proposed VCO.

coupling of the transformer corresponds to positive feedback between the top and bottom oscillators. The transistor sizes in the top cross-coupled pair are 128 µm/60 nm, and the gate length is 256 µm for the bottom cross-coupled NMOS pair. Using the NMOS transistors instead of PMOS relaxes the current requirement, which benefits from its higher mobility. Compared with low-power class-D VCOs shown in [20][27], a relatively small transistor size is implemented. Therefore, a higher oscillating frequency and a wider frequency-tuning range can be achieved.

As shown in Fig. 2.25, the top cross-coupled transistor is biased from dynamic bias control, while the oscillation frequency is tuned by a 4-bits capacitor bank using the low-level metal (M1∼M5). Both of the cross-coupled NMOS pairs share the same DC current through the center taps of both windings in the TF. A 128 µm/60 nm NMOS transistor is used in the top tanks, while the gate length of the bottom transistors is 256 µm. The current requirement is relaxed by implementing NMOS transistors as the negative resistance, which benefits from its higher mobility. The loaded resonator network shows two possible resonant frequency given by [45]

$$\omega_{\mathrm{L,H}}^2 = \frac{1+\xi \pm \delta}{2(1-k^2)}\omega_2^2 \,, \quad \text{where} \;\; \xi = \frac{L_{\mathrm{S}}C_S}{L_{\mathrm{P}}C_{\mathrm{P}}} \tag{2.26}$$

While $\omega_2^2 = (L_{\mathrm{S}}C_{\mathrm{S}})^{-1}$, $\delta = \sqrt{(1+\xi)^2 - 4\xi(1-k_m^2)}$ and the k_{m} is the coupling factor. To avoid multi-oscillation, the ξ is controlled around 1.5 to prevent large impedance peak existing at the high frequency [29]. Using the equivalent model of the TF-based network in [30], the double coupled oscillators can be implified. Thus the start-up condition and the voltage amplitude can be estimated as derived in [39]. The output amplitude from the bottom drain node can be express as

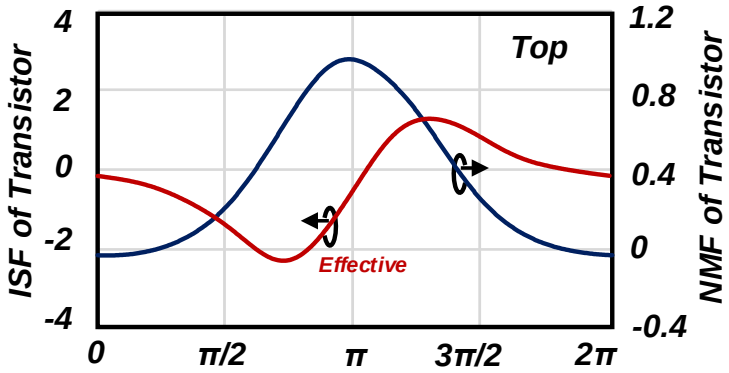
$$V_{\mathrm{AMP,VON}} \approx \frac{4}{\pi} I_{\mathrm{BIAS}} \omega_{\mathrm{L}} \frac{L_{\mathrm{P}}}{2} Q_{\mathrm{P}} \left(k_{\mathrm{m}}^2 N + k_{\mathrm{m}}^2 + \frac{L_{\mathrm{S}} Q_{\mathrm{S}}}{L_{\mathrm{P}} Q_{\mathrm{P}}} \right) \tag{2.27}$$

in which, $N = \sqrt{L_{\mathrm{S}}/L_{\mathrm{P}}}$. It must be noted that Eq. (2.25) indicates if a larger fundamental amplitude A_1 can be obtained with a minimized excessive gain G_{X}, the up-converted flicker noise will also be minimized. Eq. (2.27) indicates a larger amplitude can be obtained compared with conventional CMOS-type VCO, which benefits from a passive gain $(k_{\mathrm{m}}^2 N + k_{\mathrm{m}}^2)$. Meanwhile, we can also notice that the excessive gain G_{X} has the highest contribution as the high-order item in expression, which has been confirmed in [42]. To start the VCO, the excess gain G_{X} is usually set between 2 and 4 to guarantee a robust oscillation start-up. In this TF-based VCO, the g_{m} from both top and bottom transistors are set at around 2 ms at start-up with a 190 µA current, which given with enough margin for the oscillation in different PVT corners. The minimum oscillation power can be only 170 µA at 0.5 V in post-layout simulation, corresponding to 1.6 ms (minimum required g_{m}). A larger than 300 mV voltage amplitude can be obtained at the bottom drain node VON and VOP with 103 µW power consumption in post-layout simulation, as shown in Fig. 2.26.

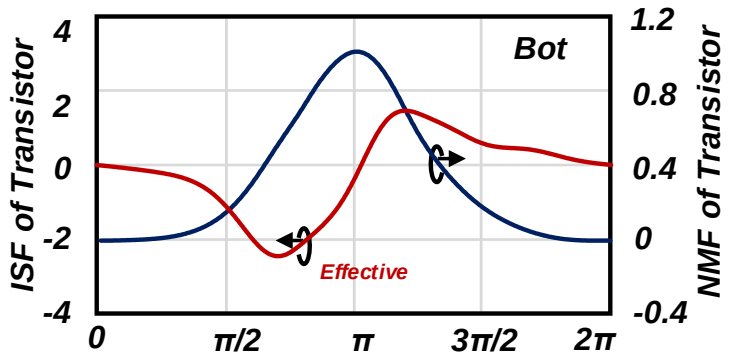
As we noticed from [39], the tail transistor will contribute most of the noise due to the insufficient V_{DS}, which makes the tail transistor working in the triode region. Meanwhile, the flicker noise of the tail transistor will modulate the oscillation amplitude and also the frequency. Thus, the flicker corner will be heavily increased from the AM-FM flicker-noise up-conversion. In this work, the tail transistor is replaced by an 8-bits digitally controlled resistor bank to control the DC current with a lower voltage headroom ($\leq$0.1 V). Thus, there is no flicker up-conversion from the tail resistors, and the flicker corner of the VCO will also be improved. The simulated impulse sensitivity function (ISF) and noise modulation function (NMF) are shown in Fig. 2.27. A similar ISF function compared with conventional class-B CMOS-type VCO can be observed in this figure.

Thanks to the large fundamental amplitude A_1 with a minimized excessive gain G_{X} and a moderate Q-factor from the TF with embedded PGS, the flicker noise up-conversion is minimized and degradation due to the current-control circuit can be avoided.

To mitigate the supply voltage variation coming from the switching DC-DC converter, a conventional LDO implementation and an amplitude tracking loop [46] in VCO design are shown in Fig. 2.24. To ensure a favorable function of the LDO or the current transistor, an extra voltage headroom (0.2 V$\sim$0.3 V) will degrade the system efficiency due to the lower voltage efficiency. Meanwhile, the additional blocks consume 0.2 mW in [46], which is unappreciated in the ultra-low-power designs. In this proposed VCO, as shown in Fig. 2.28, the DC bias of the top transistor is isolated from the cross-coupled transistor



(a)



(b)

Figure 2.27: Simulated ISF and NMF of transistors in the TF-based VCO: (a) top transistors (b) bottom transistors.

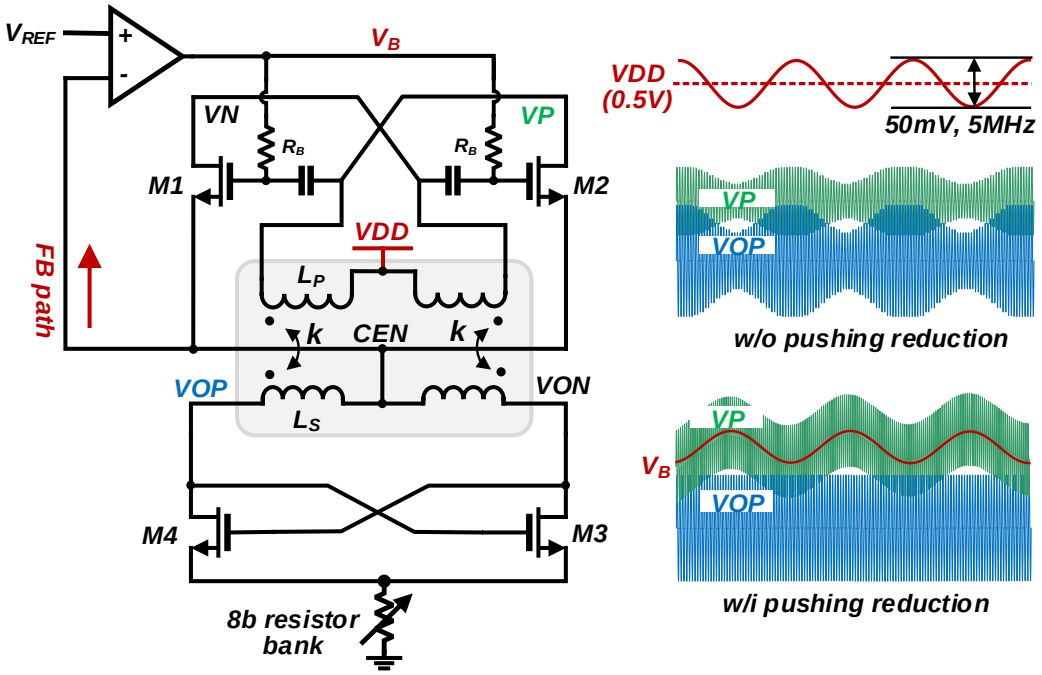


Figure 2.28: Schematic redarwn of the TF-based VCO with proposed supply pushing reduction.

using a capacitor as a DC cut. A 0.5 V VDD is directly applied at the center tap of the primary winding of the TF, while a voltage from the center tap (CEN) is fed back to an error amplifier. A PMOS-type differential to single amplifier is implemented to handle the input signal with DC level around 0.25 V. The error between the feedback voltage signal and the constant reference (V_{REF}) is amplified, and the comparison outcome will adjust the bias of the top transistor (V_{B}) to maintain constant DC current and the voltage amplitude, and thus parasitic capacitance is stabilized, which leads to a constant oscillation frequency. A 50 mV sine wave with 5-MHz frequency is added on the 0.5 V DC supply of VCO, and the error amplifier is powered by a usual 1 V DC supply. The output voltage waveform of w/wo the proposed pushing reduction loop is also shown in Fig. 2.28.

As we notice, it isn't very easy to do an accurate numerical analysis due to the transistors' time-varying non-linear behavior working in the large-signal condition. However, an equivalent model and the close-loop transfer function shown in Fig. 2.29 can be utilized to estimate the relationship between the variation of the current ΔI and other parameters in the loop. Also, the oscillation amplitude can be obtained from Eq. (2.27), which has a linear relationship with the DC current, and thus the correspondence between the variation of the DC supply and the oscillation frequency can be estimated. Meanwhile, the correspondence gives guidance for selecting the parameters in the supply pushing reduction

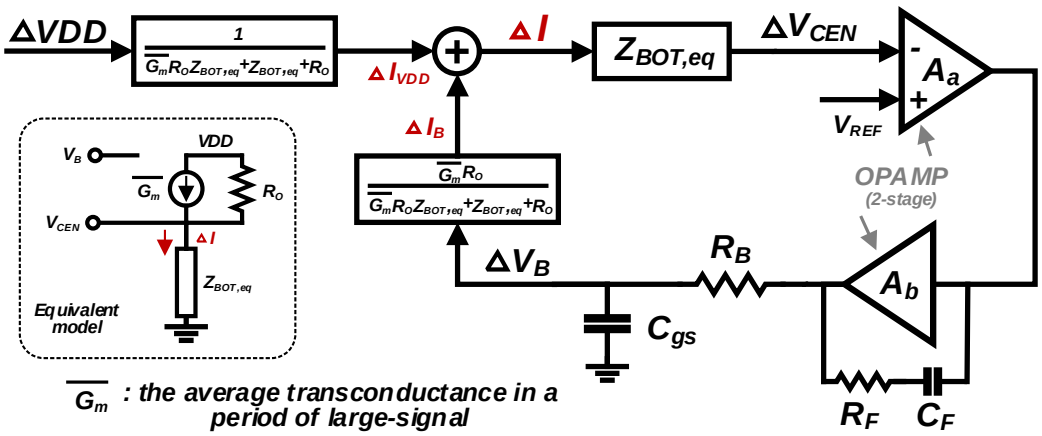


Figure 2.29: Equivalent model to qualitative analyze the supply pushing reduction loop.

loop.

According to this model, the current variation ΔI can be expressed as

$$\Delta I \approx \frac{\Delta VDD}{\left(\overline{G_{\mathrm{m}}}R_{\mathrm{O}}Z_{\mathrm{BOT,eq}}+R_{\mathrm{O}}+Z_{\mathrm{BOT,eq}}\right)+\frac{A_{\mathrm{op}}\overline{G_{\mathrm{m}}}Z_{\mathrm{BOT,eq}}R_{\mathrm{O}}}{1+SC_{\mathrm{gs}}R_{\mathrm{gs}}}} \tag{2.28}$$

where $Z_{\mathrm{BOT,eq}}$ is the large-signal equivalent impedances of both cross-coupled transistor pairs [46], while $\overline{G_{\mathrm{m}}}$ is the average effective transconductance and the R_{O} is the equivalent resistance in a period of the oscillation signal. A_{op} represents the transfer function of the error amplifier.

To minimize the power consumption of the error amplifier, the PMOS-type op-amp is constructed with two stages, which has a 60 dB open-loop gain with a 50 kHz bandwidth and more than 80° phase margin thanks to the internal series RC feedback (R_{F}, C_{F}). As we noticed from Eq. 2.28, the $\overline{G_{\mathrm{m}}}$ also enhances the gain of the feed-forward, which can reduce the gain requirement of the error amplifier. Meanwhile, all the low-frequency poles are from the error amplifier. That means a wider suppression bandwidth can be obtained from an error amplifier with large bandwidth, while considering the trade-off with power consumption. A 5 kΩ resistor is selected as the bias resistor (R_{B}) to minimize the noise contribution of this resistor, which is directly connected to the transistor's gate, and also to maximize the supply pushing suppression bandwidth without too much VCO gain penalty. Fig. 2.30 shows the simulated K_{VDD} with different frequencies of the sine wave. In the simulation, the reference voltage is generated by injecting a current from bandgap reference into an NMOS diode. The simulated worst K_{VDD} is lower than 2 MHz/V, and a 6-MHz supply pushing suppression bandwidth is achieved with an additional 40 µW power consumption from error amplifier.

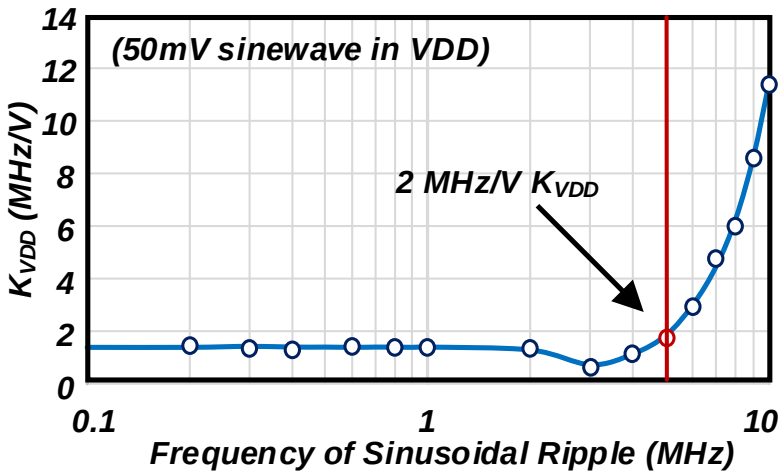


Figure 2.30: Simulated supply pushing of the VCO with different sinusoidal waveform in VDD.

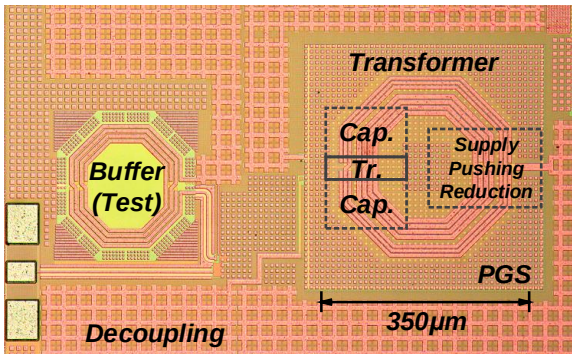


Figure 2.31: Chip micrograph.

Table 2.3: PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ULP-VCOS

	This Work	**[46]**	**[39]**	**[36]**	**[37]**	**[38]**	**[47]**
Tech. (nm)	65	40	65	180	180	28	65
Architecture	Dynamic current control	Feed-forward and calibration loop	N.A.	N.A.	N.A.	Dynamic supply control (w/i LDO)	Noise suppression loop
Oscillator Type	TF	LC	TF	LC	TF	LC	ring
Freq. range (GHz)	2.39∼2.64	4.9∼5.7	2.05∼3.10	4.5	3.8	2.35	3.2
VCO VDD (V)	0.5	1	0.45	0.2	0.5	0.5	1
Osc. Power (μW)	103	800∼1300	107	114	570	380	2.73**
Flicker Corner (kHz)	16	<100	N.A.	200∼300	N.A.	N.A.	N.A.
PN@1MHz (dBc/Hz)	-114.8	-107.9 ∼-110.9	-107	-104	-119	-115.9	-88
FOM (dBc/Hz)	-193	-185	-185	-187	-193	-187.5	N.A.
Ripple Amplitude (mV)	50	50	N.A.	N.A.	N.A.	N.A.	20
Spur (dBc)	-50.2	-58	N.A.	N.A.	N.A.	N.A.	-48
K_{VDD} (MHz/V)	2	<0.5*	N.A.	N.A.	N.A.	N.A.	4*
Pushing Reduction Power (μW)	40	200	N.A.	N.A.	N.A.	N.A.	0.456
Area (mm^2)	0.12	0.23	0.16	0.13	0.23	0.17	0.047**

*Calculated from the spur level.
**Including the whole ADPLL.

2.5 Measurement Results of The ULP VCO with Supply Pushing Reduction

The compact TF-base ULP VCO with embedded PGS and supply pushing reduction is fabricated in 65-nm CMOS technology. The chip photo shows in Fig. 2.31. Manually dummy metal filling is utilized for the density rule check and to mitigate the performance degradation. The core on-chip area is only 0.12 mm^2 with a 0.35 mm side length. Fig. 2.32 shows the measured PN performance. A -114.8 dBc/Hz PN at 1-MHz frequency offset is achieved with a 103 µW power consumption from a 0.5-V DC supply, and the corresponding FoM is -193 dBc/Hz at 2.6 GHz oscillation frequency. The frequency can be tuned from 2.39 GHz to 2.64 GHz with a 250-MHz tuning range. Thanks to the ultra-low current operation and comparatively large transistor size, the flicker corner of the proposed TF-based VCO achieves 16 kHz, which is much better than the other reported ULP-VCO designs [36][46]. The proposed TF-based VCO potentially satisfies the open-loop operation in a BLE TRX, which requires the frequency shift must be less than $\pm$50 kHz. The calculated residual FM, Δf_{FM} is 2.15 kHz according to [17] and appears to be good enough to realize a 17-ms BLE packet with the open-loop operation.

Fig. 2.33 summarizes the FoM performances of the low-power LC-VCO designs. Several works achieve excellent PN and FoM performance, but the required power consumption is still higher than 1 mW. Though some works achieve ultra-low-power operation, the phase noise performances become poor, and the FoM is limited to -190 dBc/Hz. The proposed TF-based VCO breakthrough the FoM barrier with smaller power consumption. Fig. 2.34 shows the measured spectra of the VCO with and without the supply pushing reduction. In measurement, the reference voltage is manually controlled by an adjustable off-chip LDO. A 50 mV sine ripple is added into VCO's supply to observe the effect of the proposed supply pushing reduction technique. The spur at the 5 MHz frequency offset is reduced by 18 dB and reaches -50 dBc. The performance summary of ULP-VCO is shown in Table 2.3. Compared with the state-of-the-art ULP-VCO designs, this work achieves lower power consumption within a smaller on-chip area, and the embedded supply pushing reduction also achieves good spur suppression performance with a minimized power consumption.

In this work, a miniaturized TF-based VCO is presented for IoT applications. The proposed VCO achieves a -114.8 dBc/Hz PN at 1-MHz frequency offset with a 103 µW power consumption. A -193 dBc/Hz FoM is achieved at 2.6 GHz oscillation frequency. The low-power operation and large transistor size improve the flicker corner to 16 kHz. The low-flicker noise and good $1/f^2$ PN performance allow the open-loop operation in a maximum 17-ms packet length BLE transceiver. And thus, the power efficiency of the

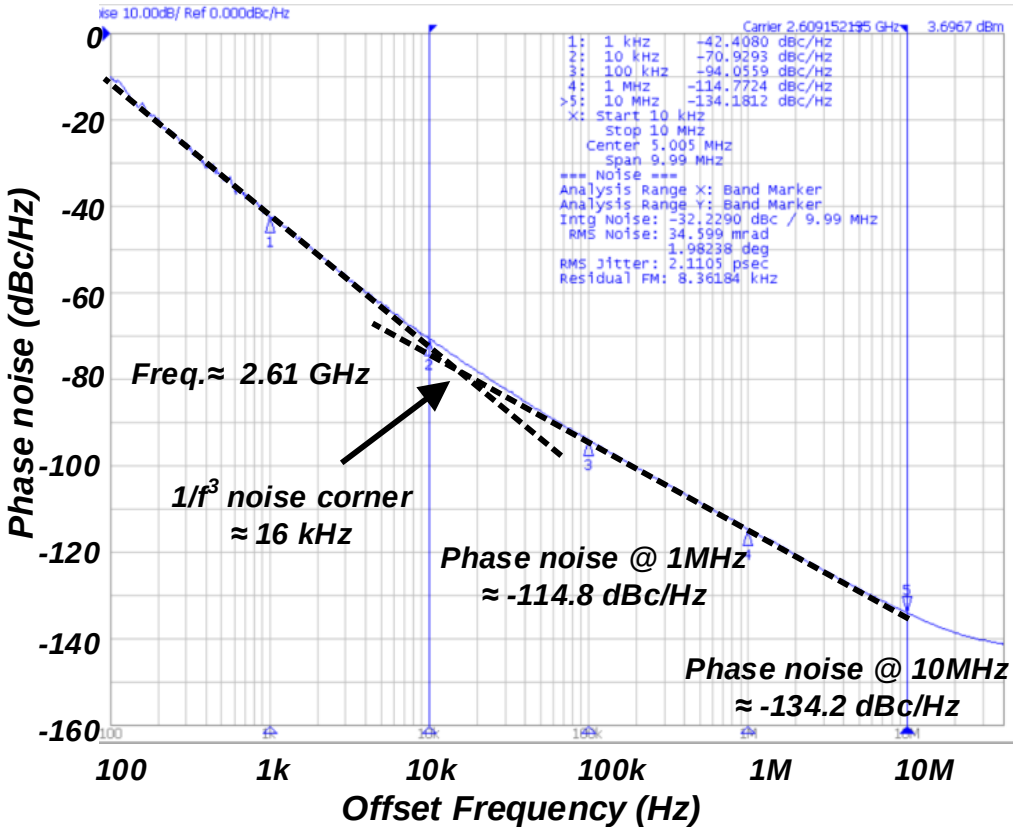


Figure 2.32: Measured TF-based VCO phase noise at 2.6 GHz oscillation frequency.

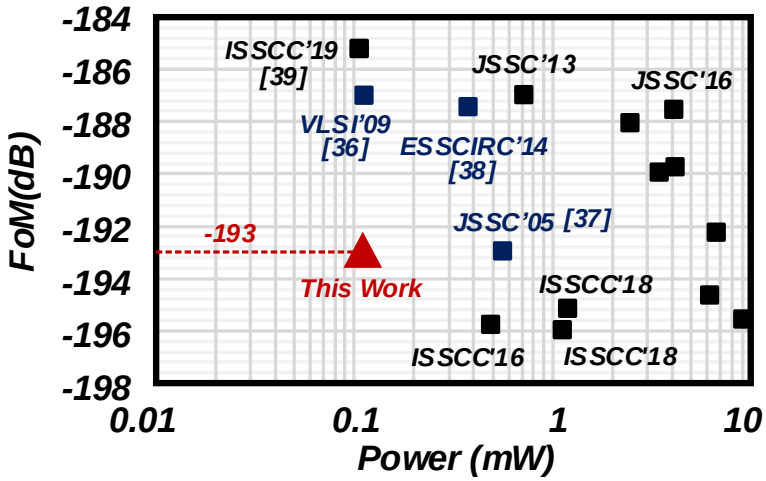


Figure 2.33: The FoM summary of state-of-the-art low-power VCO designs.

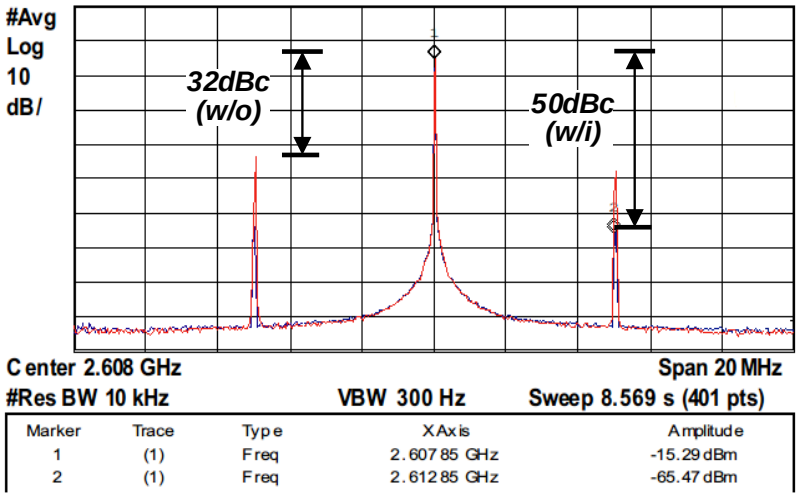


Figure 2.34: Measured oscillator spectra with and without the supply pushing reduction under 50 mV 5 MHz sine wave.

TX can be further improved with the implementation of the proposed VCO. The PGS embedded TF used in this work indicates that the compact TRX layout can be realized with a smaller on-chip area. The core area of the proposed VCO is only 0.12 mm^2, as same as the transformer. To mitigate the PN degradation from the voltage ripple introduced by the DC-DC converter in battery-powered portable devices, a supply pushing reduction loop is embedded with the VCO while consuming no additional voltage headroom. The power consumption of this loop is also minimized to 40 µW, and the supply pushing is reduced to 2 MHz/V, resulting in a -50 dBc spur with a 5 MHz sinusoidal ripples.

2.6 A High Jitter Performance Injection-Locked Clock Multiplier

This section presents a high jitter performance injection-locked clock multiplier using an ultra-low-power voltage-controlled oscillator for IoT application in 65-nm CMOS. The proposed transformer-based VCO achieves low flicker noise corner and sub-100 µW power consumption. Double cross-coupled NMOS transistors sharing the same current provide high transconductance. The network using a high-Q factor transformer provides a large tank impedance to minimize the current requirement. Thanks to the low current bias with a small conduction angle in the ULP VCO design, the proposed TF-based VCO's flicker noise can be suppressed, and a good PN can be achieved in the flicker region ($1/f^3$) with sub-100 µW power consumption. Thus, a high figure-of-merit can be obtained at both 100 kHz and 1 MHz without an additional inductor. The proposed

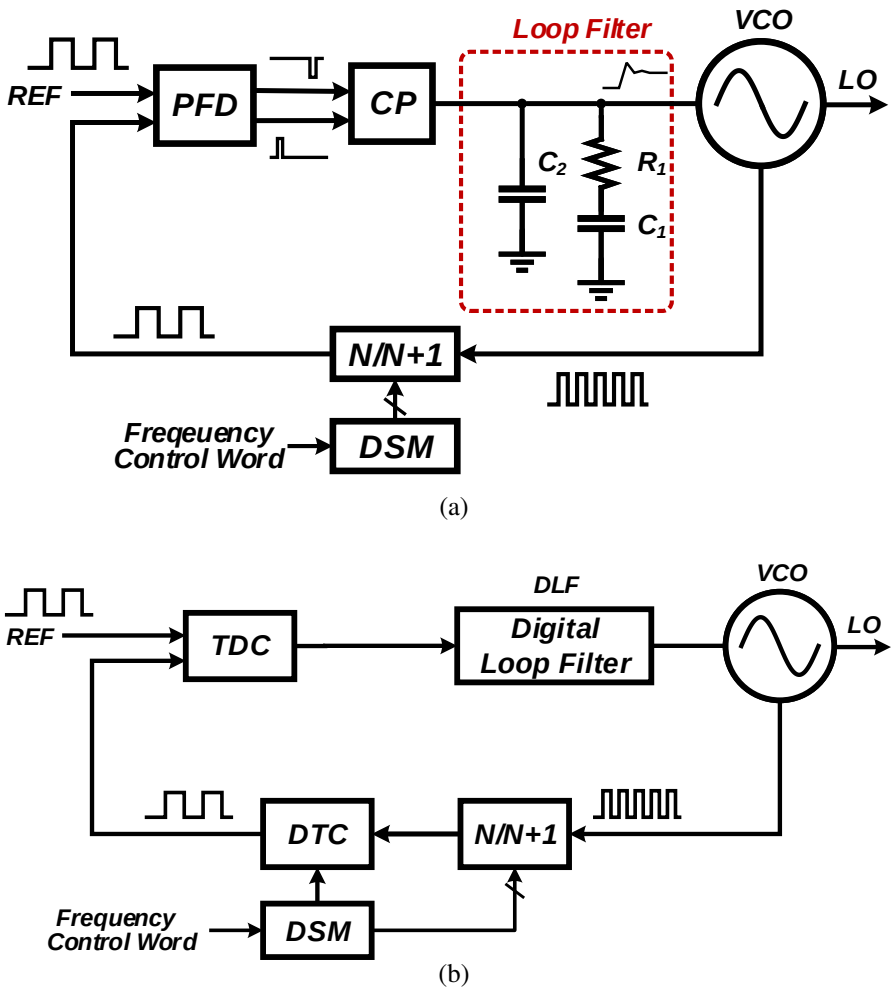


Figure 2.35: Different types of phase-locked loop (a) analog type (charge-pump based) (b) digital type.

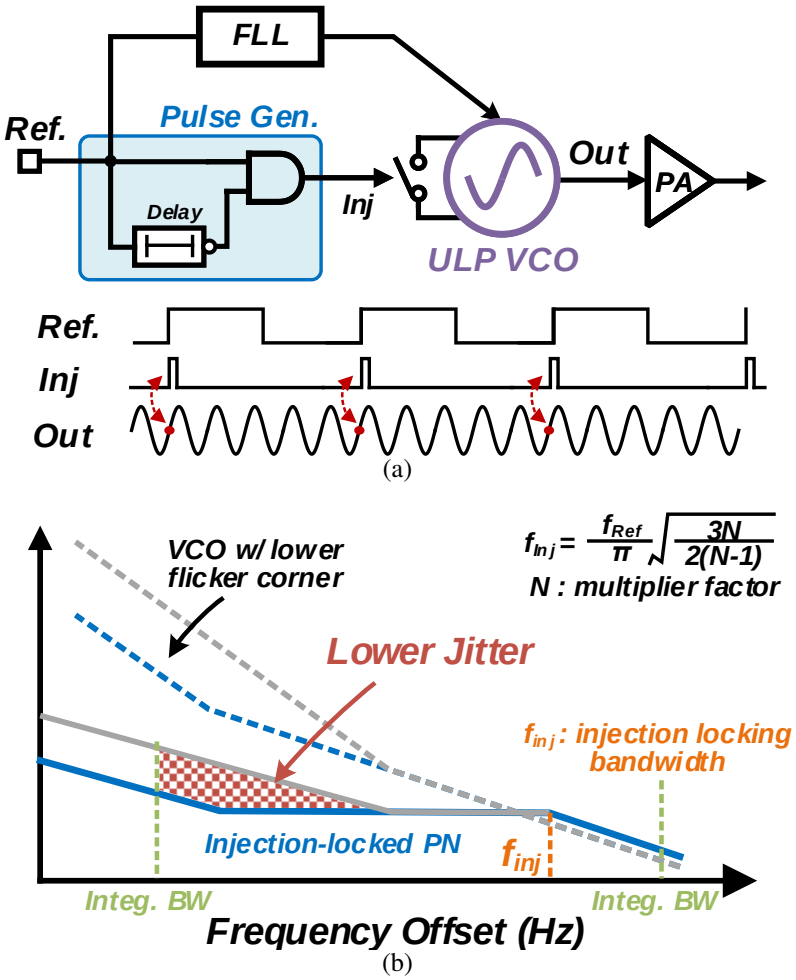


Figure 2.36: (a) Time-domain waveform during injection for frequency multiplication. (b) Frequency-domain phase noise with reference injection.

VCO achieves phase noise of -94.5/-115.3 dBc/Hz at 100 kHz/1 MHz frequency offset with a 97 µW power consumption, which corresponds to a -193/-194 dBc/Hz VCO FoM at 2.62 GHz oscillation frequency. The measurement results show that the $1/f^3$ corner is below 60 kHz over the tuning range from 2.57 GHz to 3.40 GHz. Thanks to the proposed low power VCO, the total ILCM achieves 78 fs RMS jitter while using a high reference clock. A 960 fs RMS jitter can be achieved with a 40 MHz common reference and 107 µW corresponding power.

Nowadays, the low jitter clock synthesizer is one of the most demanding components in various systems [48–51]. Those devices sustained by energy harvesters or low capacity battery must support low-voltage and low-power operation. That puts challenges on the clock synthesizer designs with considering the frequency tuning range (FTR), phase noise (PN), and power consumption. As one of the types of clock synthesizer, phase-locked

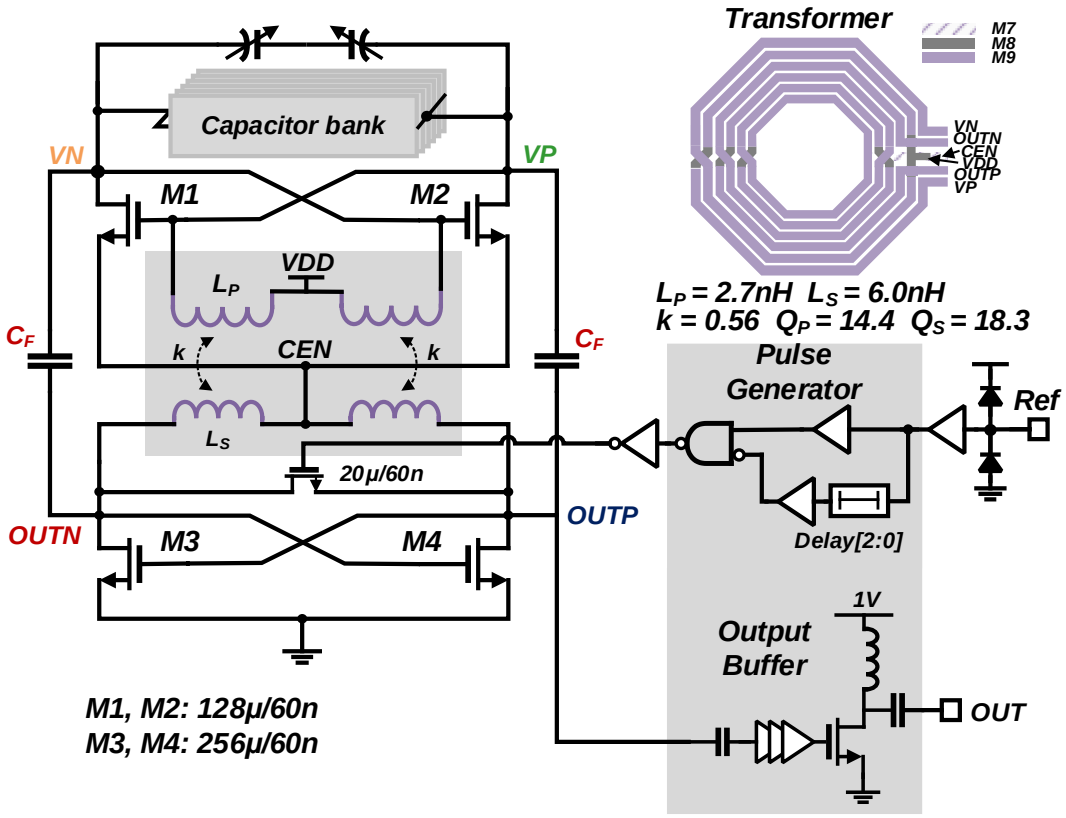


Figure 2.37: Proposed ILCM with Transformer-Based VCO.

loops (PLLs) based clock multipliers are commonly implemented in modern systems-on-chip that multiply a low-frequency reference provided by a crystal oscillator. As we noticed, the commonly implemented type-II PLLs using low reference frequency can't provide sufficient voltage-controlled oscillator (VCO) noise suppression bandwidth, *e.g.,* < 1 MHz, that protrudes the importance of $1/f$ (flicker) noise suppression in VCO, which degrades the close-in PN [52]. In contrast to PLLs, the injection-locked clock multipliers (ILCMs) lock oscillation frequency to an integer multiplier number of reference clock by injection pulses [50, 53]. In which the noise performance of the VCO, including the flicker noise, has a significant influence on the ILCM's phase noise performance.

Forwarding the reference frequency and injecting it directly into the VCO has been used to improve the jitter performance of the VCOs [54–59], which has lower power consumption benefiting from its simple structure. The conventional ILCM is shown in Fig. 2.36(a). By correcting the oscillator zero-crossings periodically using the pulse generated from a low jitter reference, the jitter accumulation can be lowered [60]. And a good in-band phase noise can be achieved thanks to the wide noise suppression bandwidth, as shown in Fig.2.36(b). According to phase noise analysis in [61], the single-sideband phase noise $\mathcal{L}_{\mathrm{IL}}(f)$ of injection-locked clock multiplier based on a VCO is given as

$$\mathcal{L}_{\mathrm{IL}}(f) = \mathcal{L}_{\mathrm{VCO}} \cdot \frac{2\pi^2(N-1)(2N-1)}{3f_{\mathrm{ref}}N^2} \cdot \frac{f^2}{1+(\frac{f}{f_{\mathrm{inj}}})^2} \tag{2.29}$$

where f_{ref} is the injection reference, N is the multiplication factor, and the f_{inj} is the injection locking bandwidth, which can be expressed as

$$f_{\mathrm{inj}} = f_{\mathrm{ref}} \cdot \frac{1}{\pi} \cdot \sqrt{\frac{3N}{2(N-1)}} \tag{2.30}$$

Based on the equation (2.29) and (2.30), several inspections can be observed. First, the in-band phase noise will experience a 1st-order suppression with a wide bandwidth f_{inj}, which is close to 0.4 times f_{ref}. Thus, with a high reference frequency and a small value of N, a wide noise suppression bandwidth f_{inj} is available. Meanwhile, at the high offset frequency, the phase noise of the injection-locked VCO is 3 dB higher than the free-running VCO. Thus, according to the above points, a low-power VCO with a good $1/f^2$ noise performance is a suitable candidate to be the high jitter performance (*e.g.,* < 100 fs) ILCM with the assistance from a high reference frequency. However, it is worth noting that the noise degradation in the injection-locked frequency generator due to the flicker noise is also significant because the injection lock operation can only suppress the VCO noise by 1st-order (2nd-order in conventional type-II PLL). A VCO with a low flicker

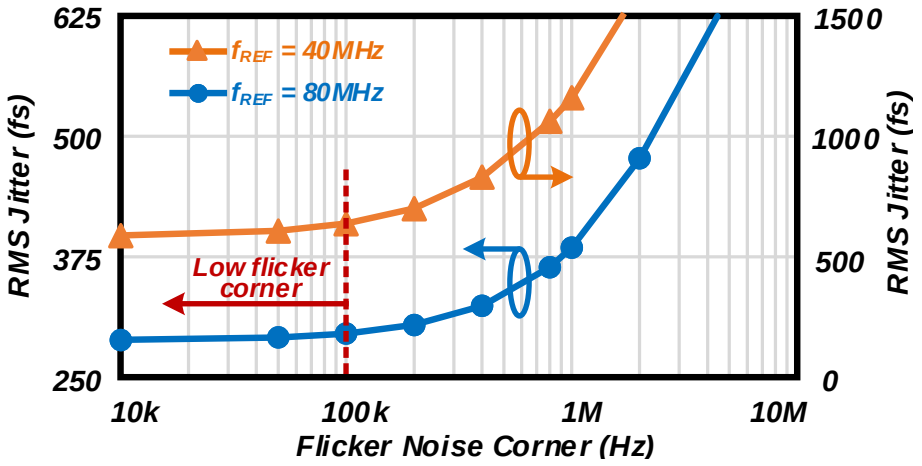


Figure 2.38: Calculated jitter performance of ILCM with different VCO flicker corner.

corner and low $1/f^2$ noise is superior compared with the one with bad phase noise performance. Fig. 2.38 shows the calculated jitter performance of the ILCM with different VCO flicker corner. In the case of a 40 MHz reference frequency, a VCO flicker corner lower than 100 kHz is desired to minimize the integrated RMS jitter with ultra-low power consumption. In addition to using a higher injection frequency, such as 80 MHz or higher, an LC-VCO, which has both good flicker noise and thermal noise performances, is attractive for high jitter performance ILCM implementation.

As CMOS scales, the MOS transistor's flicker noise will further degrade the close-in PN, thus limiting the achievable jitter performance of the PLL or ILCM and the data rate of the transceiver, finally. Since the tail filter technique [62] was firstly introduced in CMOS oscillators to suppress the $1/f$ upconversion from the current source, many efforts have been made to reducing the $1/f$ upconversion mechanisms through dedicated design techniques [63–67]. It is worth noting that these designs operate with larger than 0.3 mW power consumption. With a limited current from a low supply voltage, cross-coupled transistors with large size can provide a sufficient G_m. However, it should be noticed that the non-linear gate capacitance of the oversize transistor will increase the harmonic power and aggravate the flicker upconversion. As we know, FoM is a function of the power dissipation and the achievable phase noise performance. The VCO with ultra-low power consumption and good phase noise performance also can achieve good FoM and be attractive for low-power applications, such as digital PLL [15, 39] and BLE transceivers [11, 14]. Also, as indicated in [68], the open-loop operation of VCO can help save TX power, which requires VCO to have both low $1/f^3$ and $1/f^2$ phase noise.

In this section, a sub-100 µW VCO based on a single transformer structure is proposed with a low flicker noise corner and ultra-low power consumption, which is an extended

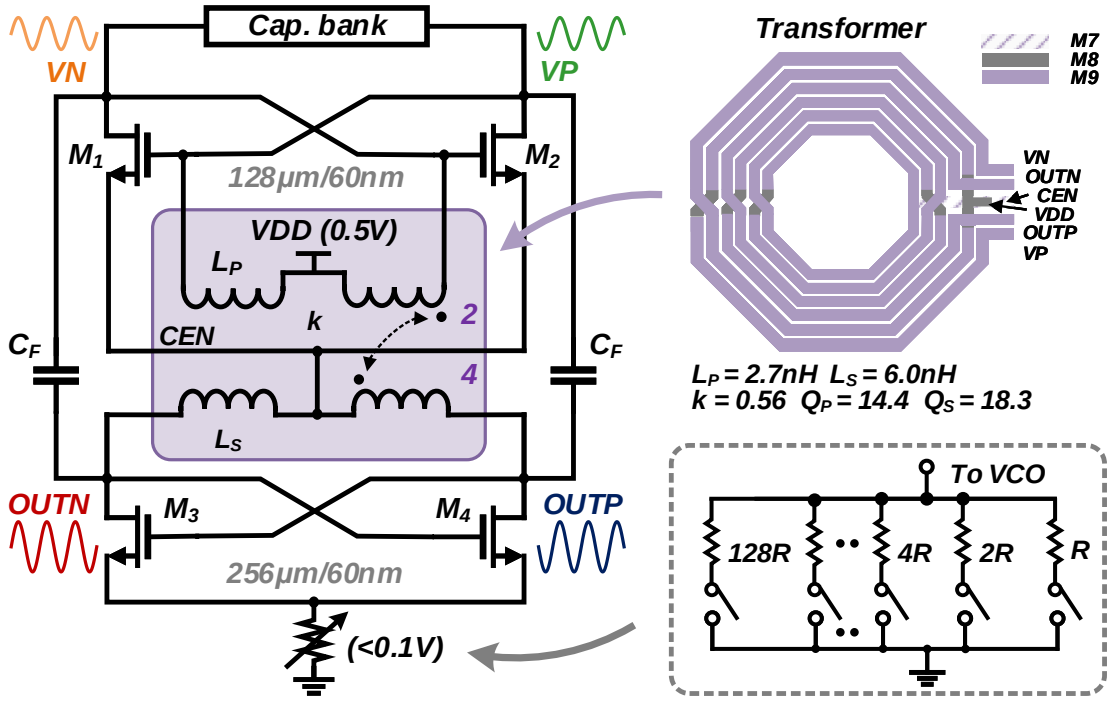


Figure 2.39: Proposed ULP transformer-based VCO with flicker noise reduction.

version of [69]. The analysis of the transformer-based tank impedance, start-up condition, and flicker noise is firstly added in this work and verified with more detailed simulation/measurement results. To verify the high performances of the VCO, a low-power ILCM is built based on this ULP VCO targeting for high jitter performance (*e.g.*, <100 fs) with sub-300 μW power consumption.

2.6.1 Transformer-Based ULP VCO

The diagram of the proposed VCO is shown in Fig. 2.39. A high-Q factor transformer using a co-planar structure is implemented in the load tank with a minimized on-chip area and a minimum number of cross-sections to achieve good PN performance with low power consumption. Also, the capacitor bank can be designed with a small tuning range with a high-quality factor (> 50) because of the large inductance of TF. Thus, the quality factor of the tank is mainly dominated by the transformer. Through the center tap of both swings, DC current is shared by the two cross-coupled NMOS transistors to provide sufficient mobility. The large inductance of the secondary swing L_S and passive gain in TF ensure the start-up with a small current bias. Both the supply port and ground port are at the bottom side of the transformer, which provides a well-defined common-mode return path.

The noise of the tail current source can appear as a CM signal and modulate the

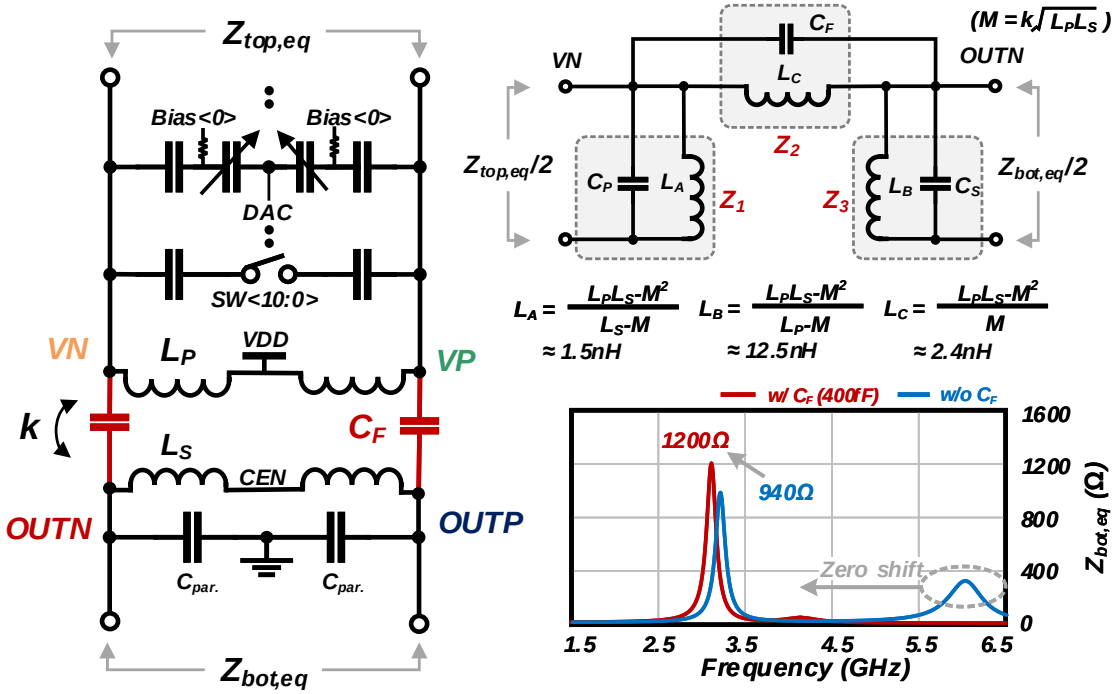


Figure 2.40: Schematic of capacitor bank and equivalent model of the half transformer.

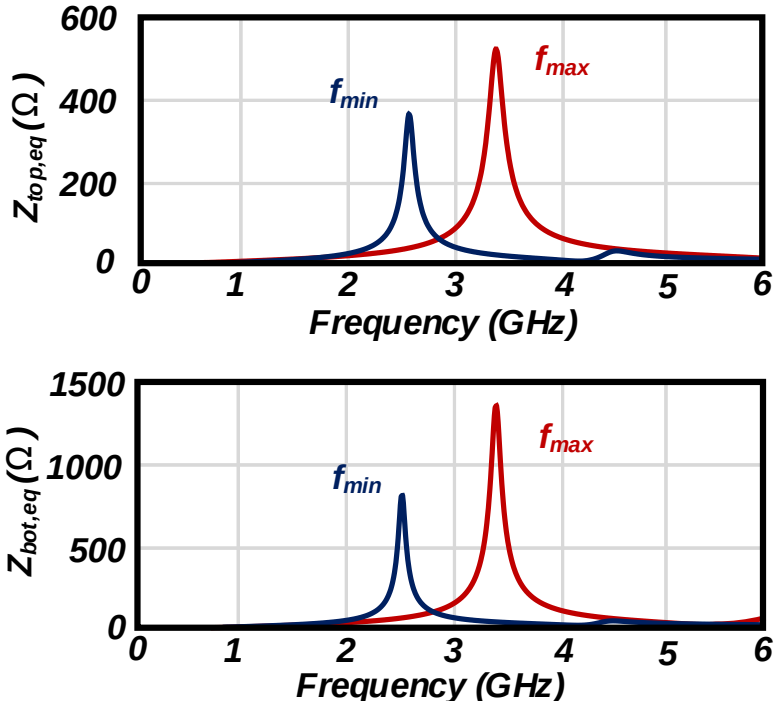


Figure 2.41: Simulated tank impedance over frequency tuning range.

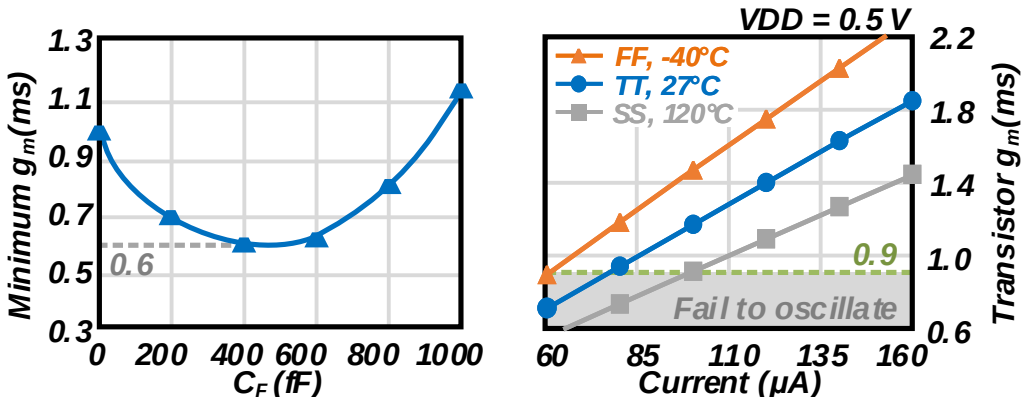


Figure 2.42: Calculated minimum required g_{m0} and simulated transistor g_{m0} versus different current bias.

oscillation voltage. This phenomenon will become more serious when insufficient voltage headroom is added to the current source [39]. Also, to mitigate the voltage drop from the current source, which degrades the voltage efficiency, an 8-bit binary resistor bank is implemented for the current control with a range from 90 μA to 360 μA.

2.6.2 Transformer-Based Tank and Start-up Condition

Fig. 2.40 shows the implemented transformer-based network with capacitor banks. A 6-bit switchable capacitor bank is implemented for coarse frequency tuning, and a 9-bit linearized varactor is used for fine frequency tuning. As derived in [39], the load impedance transfer ratio can be expressed as the turn ratio L_P:L_S and the start-up condition can be written as:

$$g_{m0} > 2/(1+L_P/L_S)Z_{bot,eq} \tag{2.31}$$

In which, $Z_{bot,\,eq}$ represents the input impedance from the bottom side of the transformer, and all the transistors (M1∼M4) have the same g_{m0} at start-up condition.

To clearly show the TF's impedance with additional C_F, the transformer's half circuit, including the VN port and OUTN port, is analyzed, and the conventional T equivalent model is converted to π equivalent model using Wye-Delta transformation [70]. Compared with T-model, the π-model shows better terminal behavior when a large leakage inductance appears [71]. The Z_1, Z_2, and Z_3 represent the parallel resonance impedance of each part in π equivalent network, as shown in Fig. 2.40.

The $Z_{bot,eq}/2$ can also be expressed as the $Z_3 \parallel (Z_2+Z_1)$. Due to the limited coupling factor k (<0.6) from the multi-turns co-planar TF structure, a large L_C appears (≈ 2.4 nH), which degrade the parallel impedance. An appropriate zero-shifting capacitance C_F [72], which resonate with L_C at fundamental frequency, can maximize $Z_{bot,eq}$ value with a slight

frequency drift. It needs to notice that the parasitic capacitance between two windings should also be considered as an additional part of C_F. To obtain a maximized impedance from bottom-side ($Z_{bot,eq}$), both of (Z_1+Z_2) and Z_3 should be maximized. In which, the value of (Z_1+Z_2) will be heavily influenced by the Z_2, which is the parallel resonate impedance of L_C and C_F. Also, because of the complexity of the actual TF model, The optimal value of C_F can only be obtained by simulation. In the simulation, a 400 fF of C_F can improve the peak impedance of $Z_{bot,eq}$ from 940 Ω to 1200 Ω which can reduce the minimum current required at the start-up condition. The simulated results of both top and bottom ports are shown in Fig. 2.41. To simulate the input impedance from the bottom-side and up-side respectively, a 50 Ω port is placed in one of the ports while the other one is floating. Note that both of the parasitic capacitance from transistors should be considered as a fixed part of the capacitor bank. The maximum oscillation frequency is achieved with the capacitor bank is turned off with approximately 210 fF capacitance, while the minimum oscillation frequency can be obtained with all the capacitors are turned on. Thanks to the high impedance $Z_{bot,eq}$ provide by this tank, the minimum required start-up g_{m0} can be minimized, and a robust oscillation start-up can be realized.

Fig. 2.42 shows the calculated minimum required g_{m0} and simulated transistor g_m versus different current bias. In simulation, a 90 µA current with 0.9 mS g_{m0} is sufficient to sustain the oscillation with a slow-slow (SS) corner (120 °C). In the post-layout simulation, larger than 300 mV oscillation amplitude is confirmed in all PVT corners with same bias current (190 µA) from 0.5 V DC supply.

2.6.3 Low flicker Noise Corner

Since the low-power start-up benefits from the cooperation of the large NMOS transistors and high tank impedance, the flicker noise upconversion is also mitigated from a small conduction angle with low-power consumption. According to the impulse sensitivity function (ISF) theory [73], the flicker noise upconversion in cross-coupled oscillation involves the following steps. First, the flicker noise, in voltage $v_{1/f}$, at the offset frequency $\Delta\omega$ will be modulated to current noise around different harmonics $k\omega_0 \pm \Delta\omega$ through a noise modulation function (NMF), which is once determined by the transistor's time-varying transconductance $G_m(t)$. It should be noted that a more accurate NMF should be utilized with the consideration of the correlated mobility fluctuation (CMF) [52], which is also influenced by the drain current I_D in advanced technology. The NMF can be described as

$$m(t) = G_m(t) + \Omega I_D(t) \tag{2.32}$$

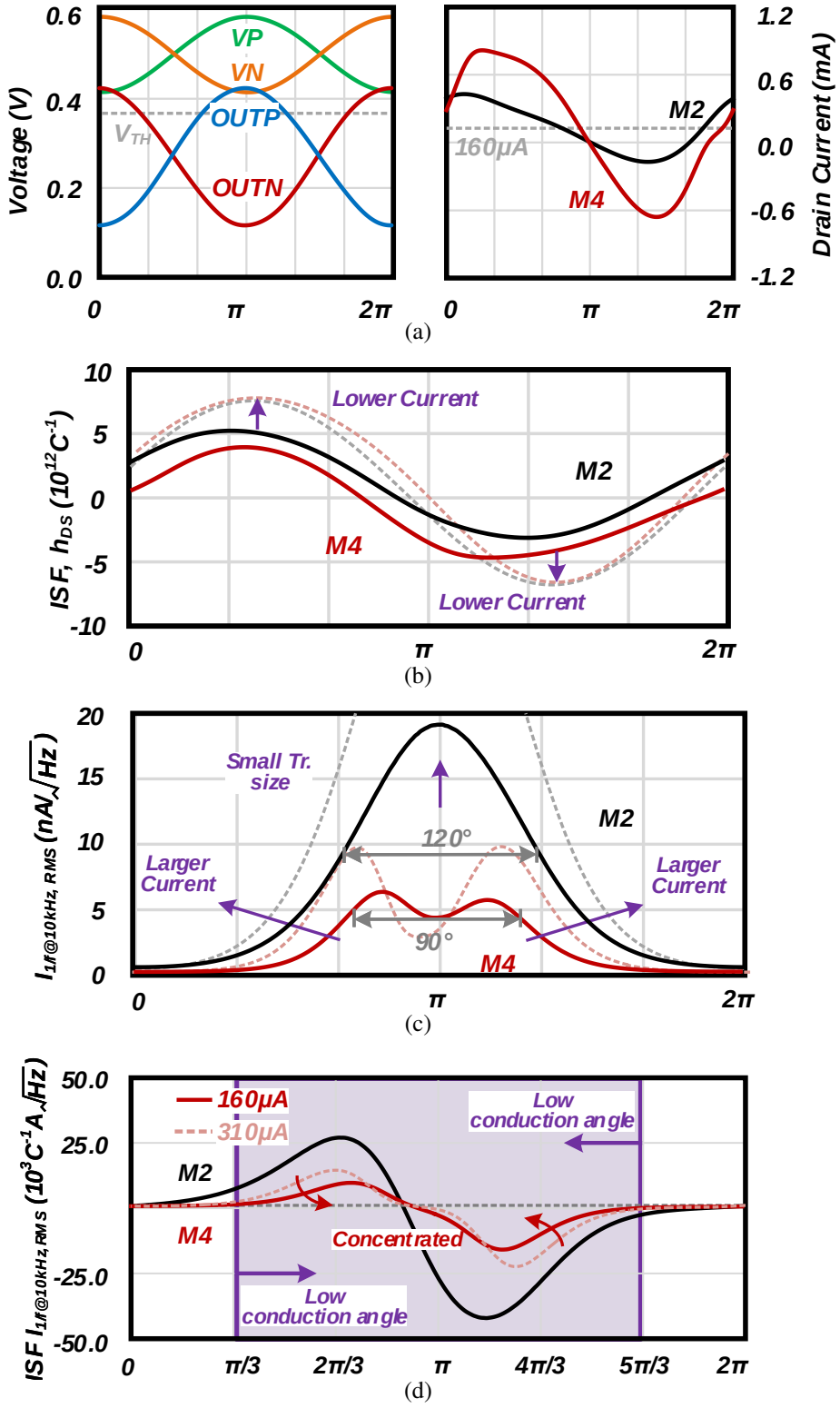


Figure 2.43: (a) Simulated waveforms of V_{GS}, V_{DS}, and drain current I_D of transistor M2 and M4. (b) Simulated Non-normalized ISF functions of M2 and M4. (c) Modulated RMS value of flicker current noise at 10 kHz of M2 and M4. (d) Simulated effective non-normalized ISF function with different current bias (160/310 μA).

where $m(t)$ is the NMF. Ω is the process parameter, which is the function of Coulomb scattering coefficients, the volumetric oxide trap density, and oxide capacitance per unit area of the interfaces [74]. $G_{\mathrm{m}}(t)$ and $I_{\mathrm{D}}(t)$ are the steady-state waveform that can be obtained by the transient simulation in Spectre. The flicker current noise can be written as

$$i_{1/f}(t) = v_{1/f}(t) \times m(t) \tag{2.33}$$

Assuming the $v_{1/f}(t)$ at $\Delta\omega$ is expressed as $v_{1/f}(t) = \sqrt{2}V_{1/f,RMS}\cos(\Delta\omega t + \gamma)$, in which the γ is an initial random phase. The current noise can be rewritten as

$$\begin{aligned} i_{1/f}(t) &= \sqrt{2}V_{1/f,RMS} \times m(t) \times \cos(\Delta\omega t + \gamma) && (2.34)\\ &= \sqrt{2}I_{1/f,RMS}\cos(\Delta\omega t + \gamma) && (2.35) \end{aligned}$$

Though the $I_{1/f,RMS}$ can be directly obtained by the periodic steady-state (PSS) simulation in Spectre, the understanding of how the $m(t)$ influences the $I_{1/f,RMS}$ can give us the guideline to design the VCO with lower flicker noise corner. According to [74], the term of ΩI_{D} is relatively small compared with the G_{m}, due to the small CMF factor Ω in 65 nm node and low current bias. Therefore, it should be noted that $G_{\mathrm{m}}(t)$ will dominate the $m(t)$ and mainly considered here.

Secondly, the flicker noise current will be converted to phase noise through its corresponding ISF, and the non-normalized ISF can be expressed as

$$h_{\mathrm{DS}}(t) = \frac{1}{2}h_0\cos\theta_0 + \sum_{1}^{N}(h_k\cos k\omega_0 t + \theta_k) \tag{2.36}$$

where h_{k} is the magnitude of the ISF at each harmonic and its corresponding phase θ_k. Both the h_{k} and θ_k can be estimated by using the simulator PSS and PNOISE in Spectre. Finally, the single-sideband to carrier ratio (SSCR) can be expressed using the non-normalized effective ISF ($h_{eff}(t)$) as

$$\begin{aligned} \mathcal{L}_{\Delta\omega} &= 2\left(\frac{\sqrt{2}}{2\Delta\omega}\cdot h_{eff}(t)\right)^2 && (2.37)\\ &= 2\left(\frac{\sqrt{2}}{2\Delta\omega}\cdot\frac{1}{T}\int_0^T h_{\mathrm{DS}}(t)\cdot I_{1/f,RMS}(t)dt\right)^2 && (2.38) \end{aligned}$$

From equation (2.38), two approaches are indicated to minimize the flicker noise corner. One is to make the $h_{\mathrm{DS}}(t)$ more symmetrical and narrow the upper and lower ranges, such as increasing the quality factor of the tank or reducing the even harmonic compo-

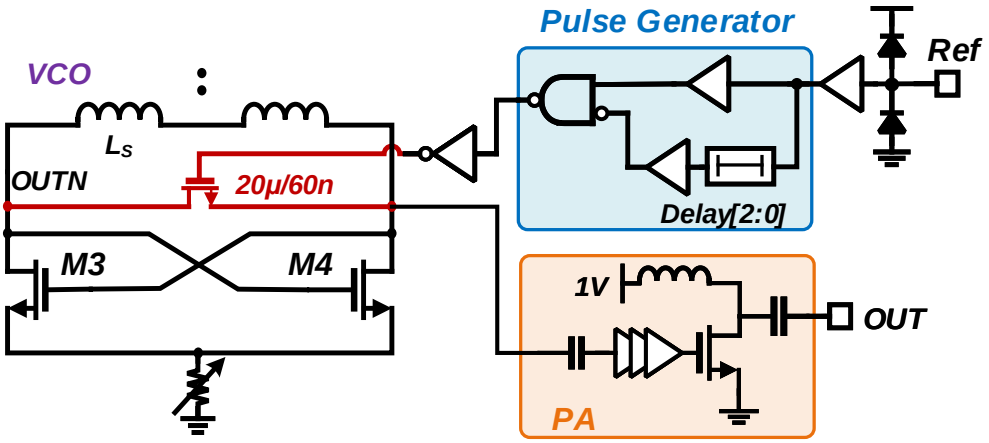


Figure 2.44: ILCM implementation with a pulse generator and test buffer.

nents. Another way is to reduce the absolute value of the $I_{1/f,RMS}$, such as increasing the transistor gate size (lower $V_{1/f,RMS}$) and narrow the conduction angle (lower $m(t)$).

In general, the flicker noise current will modulate the waveform within a window $m(t)$ determined by current and transconductance, which is influenced by the transistor's conduction angle. Thus, to reduce the flicker noise upconversion, one way is directly reduce the flicker noise current associated with the transistor's gate area. And another way is to reduce the conduction-angle (*i.e.,* class-C VCO), which also means to narrow the noise modulation window [67]. What should be noticed here is that to reduce the conductance angle in steady-state, the current bias must be relatively small to avoid a large voltage waveform. However, the small current bias will also lead to a small mean value of transconductance, which makes the start-up become more difficult [75].

Fig. 2.43(a) shows the simulated waveforms of top transistor M2 and bottom transistor M4. Due to the low supply voltage (*i.e.,* 0.5 V), which shared by the stacked structure, and the low current bias condition, the gate voltage waveform of bottom transistors is lower than the threshold voltage at most of the time. Thus, the bottom transistor cross-coupled pair works most of the time in the class-C region with a small conduction-angle ($\approx 90°$). Meanwhile, the top cross-coupled pair works with a relatively larger conduction-angle ($\approx 120°$). The flicker noise contribution from both top and bottom transistors will be mitigated. The DC value of the impulse sensitivity function accounts for the flicker noise upconversion. To verify the different current cases, both ISF and flicker noise current simulations are carried out with different current conditions. Fig. 2.43(b) shows the simulated ISF functions with different current conditions for both transistors M2 and M4. Fig. 2.43(c) shows the simulated RMS value of flicker noise current of both upper and lower transistors. With a large current that leads to a large conduction angle, the flicker noise current will increase as the red dot line shown in Fig. 2.43(c). Meanwhile,

a small transistor size will also contribute to a larger flicker noise component. As shown in Fig. 2.43(d), the effective non-normalized ISF function of M2 transistor is also small thanks to the large transistor size (128 µm/60 nm), which reduces the absolute flicker noise current. Meanwhile, the bottom transistor M4 has a much lower DC value of ISF function thanks to the narrow conduction angle with a proper current biasing. The resistor bank only degrades the $1/f^2$ phase noise in a small value ($<5\%$) and has negligible impact on the flicker corner.

2.6.4 ILCM Implementation

To indicate the performances of the proposed VCO, an ILCM diagram with an integer mode is constructed as shown in Fig. 2.44. Note that the power consumption of the VCO core and the pulse generator are commonly considered in the ILCM designs, and higher reference frequency will inevitably increase the power consumption of the pulse generator.

The pulse generator generates a narrow pulse with adjustable pulse width using the positive edges of the reference clock, and the generated pulses are injected into the TF-based VCO through an NMOS transistor [76]. The pulse width can be adjusted from 45 ps to 186 ps using a 3-bit delay control word with a 1-V power supply in post-layout simulation. A 20 µm/60 nm NMOS transistor is implemented as the shunt transistor for the pulse injection. It should be noticed that the injection from the bottom side of the VCO has a much more obvious effect because of the larger differential waveform amplitude. An inverter driven common source power amplifier is constructed as the test buffer. The first stage of the VCO buffer is using a resistor feedback low-VT inverter.

2.6.5 Measurement Results of ILCM

The phase noise is tested with a signal source analyzer (Keysight E5052B), and Fig. 2.46 shows the measured PN at 100 kHz, 1 MHz, and 10 MHz, at 2.62 GHz oscillation frequency. In measurement, two external low-dropout linear voltage regulators (LDOs) are utilized to provide an ultra-low-noise DC supply and frequency tuning voltage, respectively. Fine current control can be realized with the on-chip 8-bit resistor bank, which is added to the tail of VCO. The measured $1/f^3$ corner is 18 kHz with drawing 194 µA current from 0.5 V DC supply. Meanwhile, this proposed TF-based VCO achieves -94.5/-115.3 dBc/Hz at 100 kHz/1 MHz frequency offset, corresponding to a -193/-194 dBc/Hz VCO FoM. The difference in FoM at 100 kHz and 1 MHz is less than 1 dBc/Hz thanks to the low $1/f^3$ corner achieved in this design.

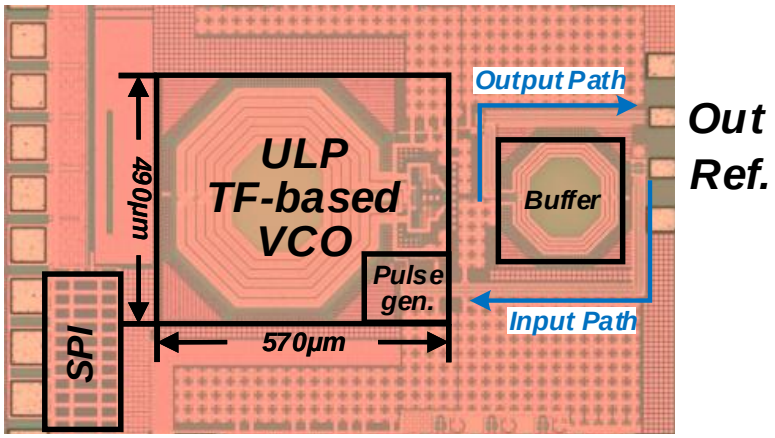


Figure 2.45: Chip micrograph.

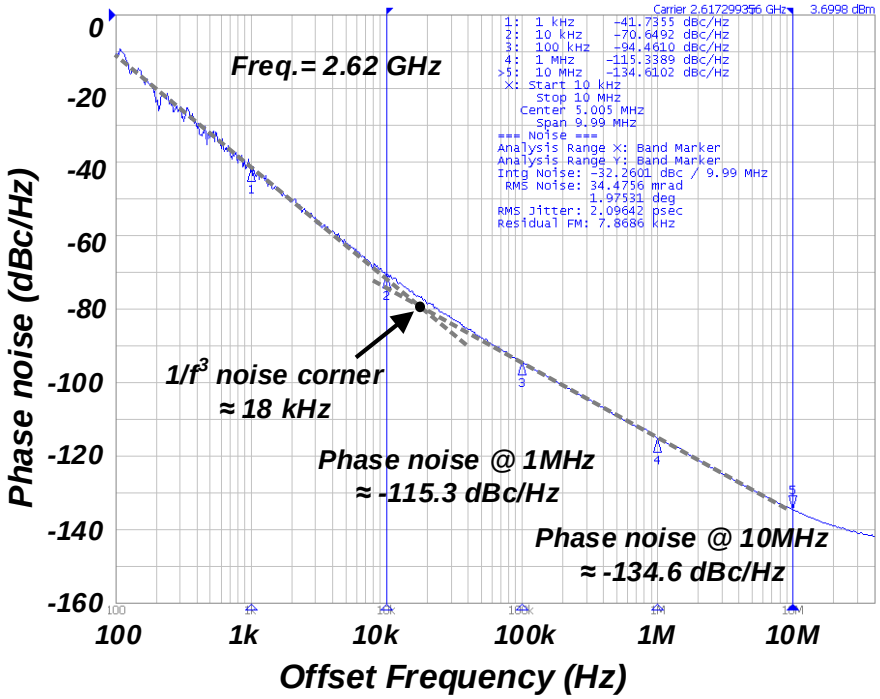


Figure 2.46: Measured phase noise of the VCO at 2.62 GHz oscillation frequency.

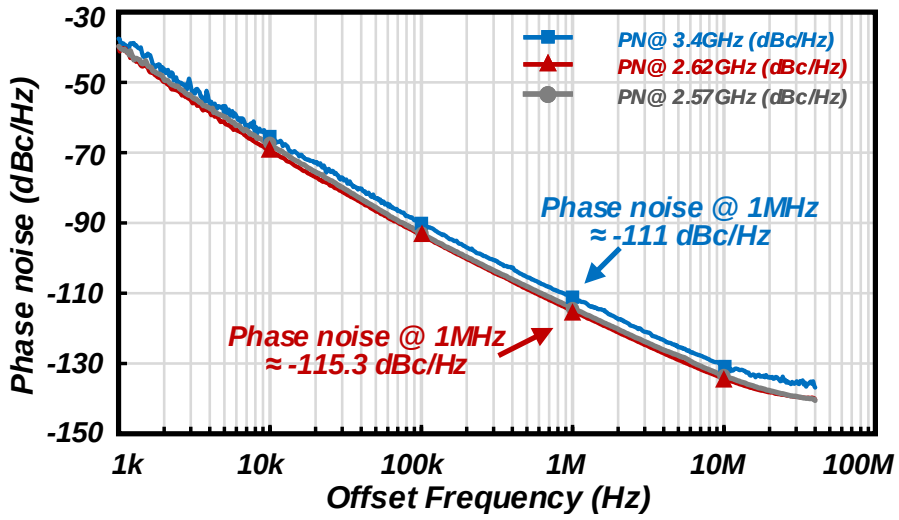


Figure 2.47: Measured phase noise of the VCO at representative frequencies.

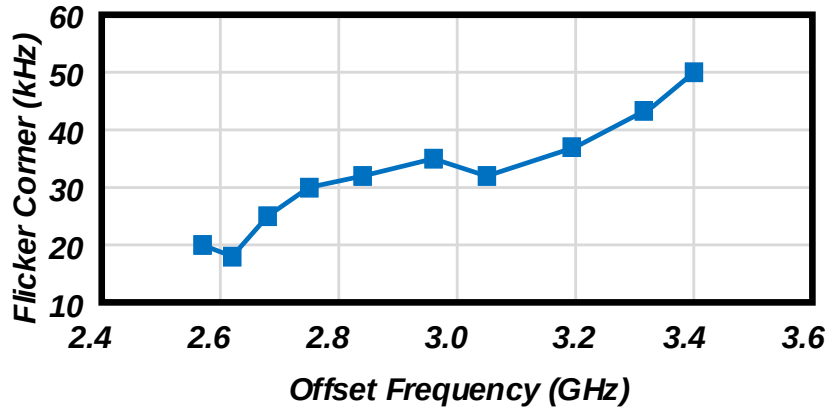
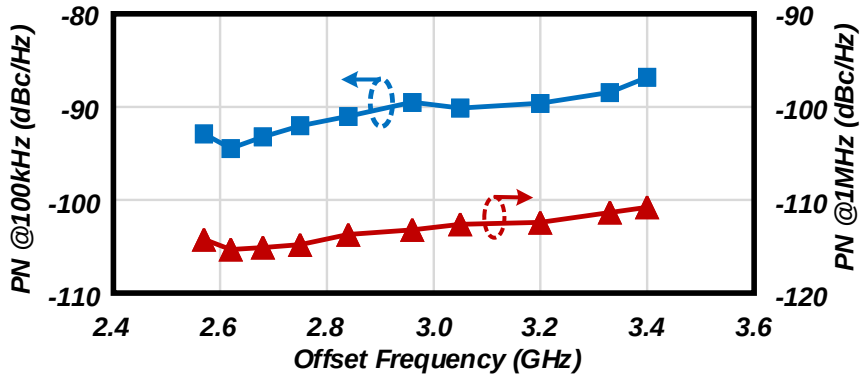


Figure 2.48: Measured flicker noise corner over the frequency tuning range frequencies.

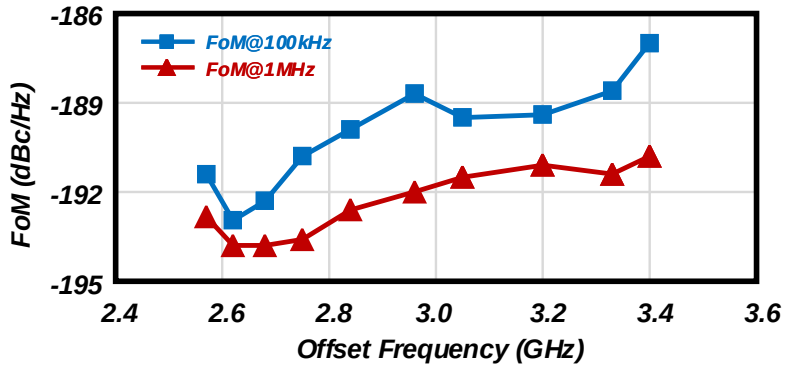
Table 2.4: PERFORMANCE COMPARISON WITH STATE-OF-THE-ART OSCILLATORS

		This Work	[65]	[67]	JSSC'13	[64]	[66]	[63]	VLSI'09
Tech. (nm)		65	28	28	65	65	40	130	180
Architecture		Implicit Resonate	Implicit Resonate	Conduct Angle Reduction	Drain Resistor	Inverse Class-F	Implicit Resonate	Noise Circulating	Dual Class-C
VDD		0.5	0.7	0.3	1.2	0.6	1.0	1.2	0.2
Tuning Range (GHz)		2.57∼3.40 (27.8%)	4.7∼5.4 (13.8%)	2.02∼2.87 (35%)	3.3∼3.6 (18.2%)	3.49∼4.51 (25.5%)	5.4∼7 (25.8%)	2.04∼2.47 (19%)	N.A.
Power (mW)		0.097	0.5	0.75	0.72	1.14	10	2.58	0.114
Osc. Frequency (GHz)		2.62	4.7∼5.4	2.4	3.3	4.51	7	2.35	4.5
Phase Noise (dBc/Hz)	100 kHz	-94.5	-108	-95.9	-47@1 kHz	-98.5	-102.1	-109.8	-79
	1 MHz	-115.2	-131	-119.3	-114	-143.7	-124.5	-131.6	-104
FoM_{VCO}* (dBc/Hz)	100 kHz	-193	-193 (@200 kHz)	-184.8	-179@1 kHz	-191	-188.9	-193.1	-181
	1 MHz	-194	-196 (@5 MHz)	-188.1	-189.8	-196.2	-191.4	-195.6	-187
Flicker Noise Corner (kHz)		18∼50	200	60∼100	N.A.	300	60	50	200∼300
TF/Inductor Count		1	1	1	1	1	1	1	1
Area (mm^2)		0.28	0.18	0.14	0.08	0.22	0.13	0.36	0.19

* $FoM_{VCO} = \mathcal{L}(f_{offset}) - 20\log(f_0/f_{offset}) + 10\log(P_{DC}/1\text{ mW})$



(a)



(b)

Figure 2.49: (a) Phase noise (b) FoM at 100 kHz and 1 MHz over the frequency tuning range frequencies.

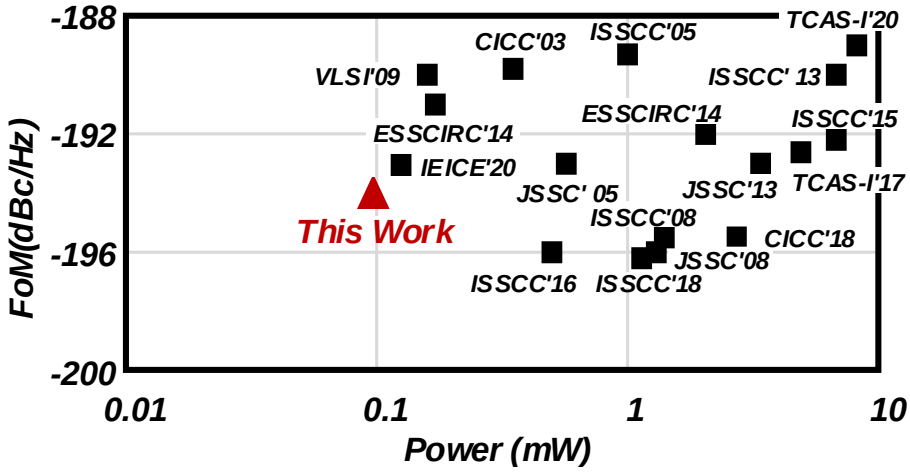


Figure 2.50: Comparison of power and FoM in low-power LC-VCOs.

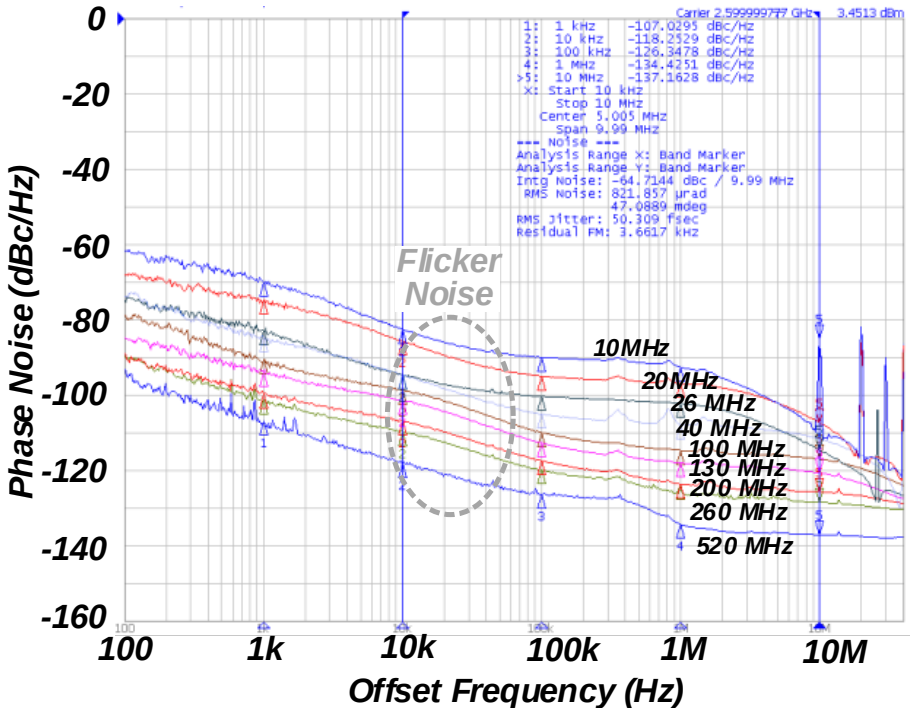


Figure 2.51: Measured injection-locked phase noise with different reference frequencies.

The PN plots at representative oscillation frequencies are shown in Fig. 2.47. The phase noise variation is lower than 4.5 dB over the frequency tuning range (FTR) from 2.57 GHz to 3.40 GHz with a peak FoM -194 dBc/Hz. The measured flicker noise corners over the frequency tuning range are shown in Fig. 2.48. The $1/f^3$ corner is below 60 kHz over the tuning range, and better flicker noise performance achieved with lower oscillation frequency. The phase noise and FoM over the frequency tuning range are summarized in Fig. 2.49. Fig. 2.49(a) shows PN at 100 kHz and 1 MHz, respectively versus different oscillation frequencies. Fig. 2.49(b) shows the corresponding FoM versus oscillation frequencies and the FoM achieves below -190 dBc/Hz over the tuning range thanks to good phase noise performance with low power consumption. The measured VCO supply sensitivity K_{VDD} is around 270 MHz/V at 0.5 V supply voltage due to the large size of transistors working in the current limited region. Fig. 2.50 summarizes the power and FoM of the low-power LC-VCO designs. This work breakthrough the sub-100 µW power barrier and achieves the best FoM around the left corner in the FoM Summary. The performance of the proposed VCO is summarized and compared with state-of-the-art VCO in CMOS processes, as shown in Table 2.4. Compared to other VCOs, this design achieves both a low flicker corner and a good $1/f^2$ phase noise performance with ultra-low power consumption.

Fig. 2.51 shows the measured injection-locked phase noise with different reference

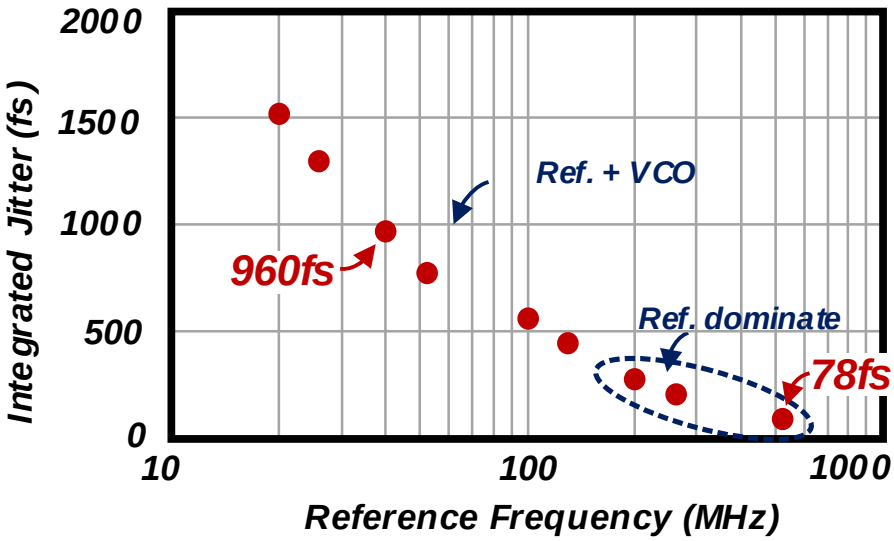


Figure 2.52: Measured integrated jitter performance.

frequencies. The ILCM is fabricated in 65-nm CMOS technology. At the 2.6 GHz operation frequency, the available injection ratio ranges from 5 to 260, corresponding to the power consumption from the 210 µW to 107 µW.

As shown in Fig. 2.52, a 78 fs integrated RMS jitter (10 kHz to 40 MHz) can be achieved with a 520-MHz reference. With a 40 MHz common reference, a 960 fs RMS jitter can be achieved with 107 µW corresponding power. Fig. 2.53 plots the calculated jitter-power FoM (FoM_{JP}), where

$$FoM_{\text{JP}} = 10\log_{10}\left\{\frac{Jitter^2}{(1\,s)^2}\cdot\frac{Power}{1\,mW}\right\} \tag{2.39}$$

The FoM with considering reference frequency, FoM_{JRP}, can be written as [77], where

$$FoM_{\text{JRP}} = 10\log_{10}\left\{\frac{Jitter^2}{(1\,s)^2}\cdot\frac{Power}{1\,mW}\cdot\frac{f_{\text{ref}}}{100\,MHz}\right\} \tag{2.40}$$

In which, the f_{ref} represents the frequency of reference clock. Fig. 2.54 compares the measured jitter performance and the power consumption of the proposed ILCM with state-of-the-art low-jitter PLLs. Table 2.5 summarizes the proposed ILCM performance and shows a performance comparison with the other works. This work achieves -50 dBc reference spur in measurement which can potentially satisfy some wireless transceivers, such as Bluetooth Low-Energy, which requires a spur level lower than -40 dBc above 3 MHz frequency offset [11]. Compared with [77], this work has a worse reference spur level due to the lack of PLL, which helps in injection timing optimization. To improve the reference spur performance, a continuous frequency tracking loop with a gated option can be

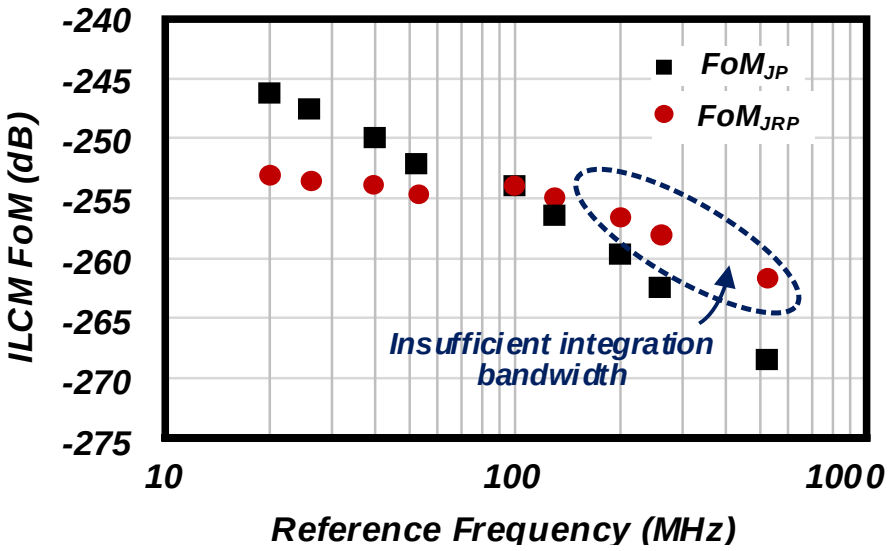


Figure 2.53: Calculated FoM with different injection reference frequencies.

Table 2.5: COMPARISON WITH STATE-OF-THE-ART WORKS.

Reference	[54]	[57]	ISSCC'14	[77]	This Work
Architecture	Int.-N ILCM	Int.-N ILCM	Int.-N ILCM	Int.-N ILCM	Int.-N ILCM
Technology [nm]	65	65	65	65	65
Freq. Range [GHz]	0.5-1.6	6.75-8.25	2.4	2.2-2.6	2.57-3.40
Multi. Factor [N]	4-30	64	16	3-24	5-260
Ref. Frequency [MHz]	40-300	105-129	150	100-800	10-520
RMS Jitter [fs] @ Ref. [Hz] (Int. Range [Hz])	700 @300M (10k-40M)	184 @106.25M (10k-100M)	188 @150M (1k-40M)	70 @800M (10k-40M)	78 @520M (10k-40M)
Ref. Spur [dBc]	-46	-40	-49	-66	-50
Power [mW]	0.97	2.25*	5.2*	0.2	0.21
Area [mm^2]	0.022	0.25	0.12	0.25	0.28
FoM$_{JP}$ [dB]	-243	-251	-247	-270	-269
FoM$_{JRP}$ [dB]	-239	-251	-246	-261	-262

* Total power of PLL, including the buffer and digital.

implemented to optimize the injection timing with PVT variations [57, 78].

2.7 Conclusion of ILCM

An ultra-low-power TF-based VCO with flicker noise reduction and good $1/f^2$ phase noise is proposed for IoT application. The transformer-based network provides a large

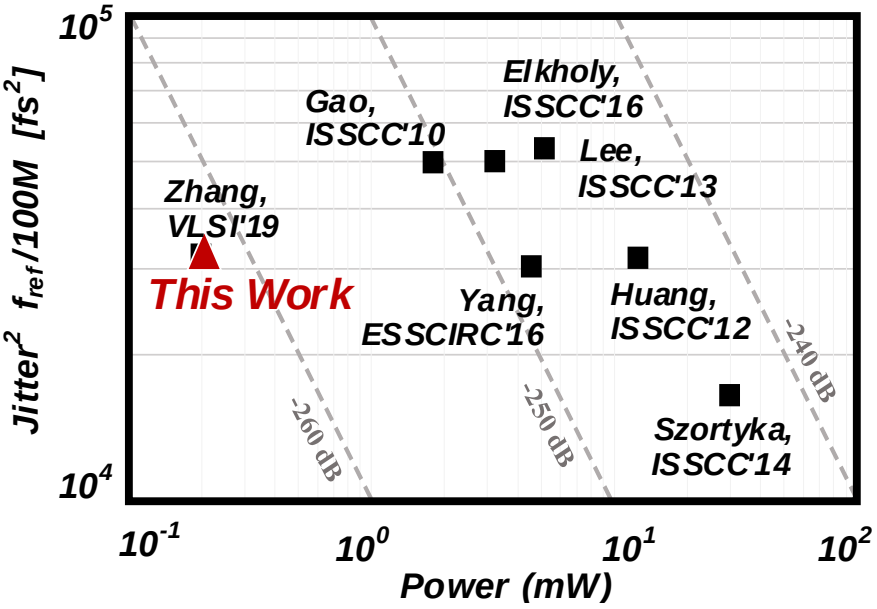


Figure 2.54: State-of-the-art ILCMs.

tank impedance with assistance from the inserted capacitor. Thanks to the high-quality factor with large tank impedance, the proposed VCO achieves -115.3 dBc/Hz phase noise at 1 MHz frequency offset while only consumes 97 µW power, which corresponds to a -194 dBc/Hz FoM. Meanwhile, an 18 kHz flicker noise corner is achieved with small current bias and conduction angle reduction, and $1/f^3$ corner is below 60 kHz over the wide tuning range from 2.57 GHz to 3.40 GHz. The proposed ULP TF-based VCO proves its feasibility in low power consumption applications with a low reference frequency. The total power of ILCM can be reduced to 107 µW, while 960 fs RMS jitter, and -254 dB FoM_{JRP} can be achieved with a 2.6 GHz operating frequency using a 40 MHz input reference clock. A 78 fs RMS jitter is also available with a 520 MHz input reference clock. The proposed ILCM demonstrates its applicability in high jitter performance and low-power clock generator applications.

Chapter 3

Bluetooth Low Energy Transceiver with Direct Antenna Interface

In the IoT era, ubiquitous sensors and devices connected through wireless modules are becoming widely used. As the strongest candidate for a wireless interface, the Bluetooth Low Energy® (BLE) standard has been already widely integrated into smartphones and wearable devices. A small and low-power BLE module, within a compact package size, is extremely attractive for disposable or highly integrated portable devices. Meanwhile, with a direct 50 Ω single-ended antenna interface, the PCB area, and cost can be significantly reduced. Therefore, a low-power and area-efficient BLE transceiver, with fully on-chip integrated matching and T/R switch function, is highly demanded for long battery life and low-cost application.

More challenges come when we consider improving the link budget of the BLE system with on-chip integration. The key performances of power amplifier (PA), low-noise

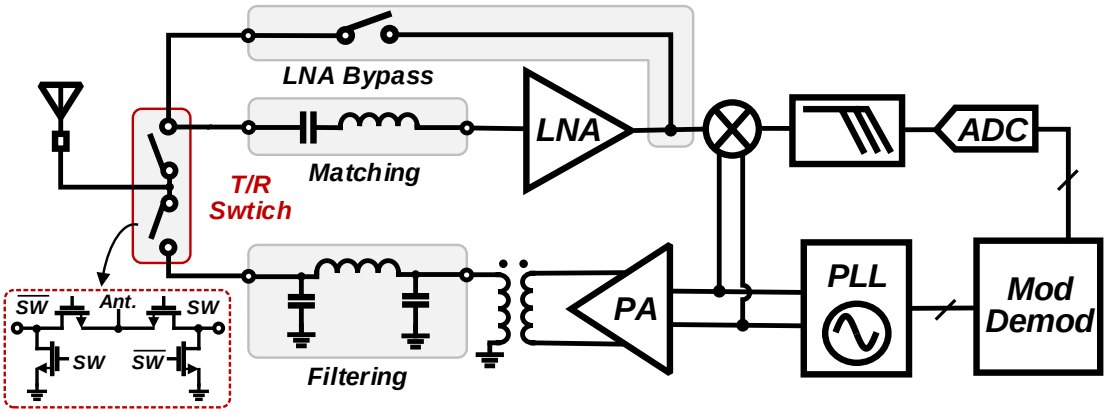


Figure 3.1: BLE transceiver with conventional SPST/SPDT switch and on-chip matching network.

amplifier (LNA), and T/R switch are difficult to be designed as the counterparts by using off-chip components due to the low-quality factor of on-chip inductors/transformers and non-ideal transistor characteristics. A conventional SPST/SPDT CMOS switch [79–81] without a diplexer can be applied in BLE TRXs owing to its time-division operation, as shown in Fig. 3.1. Obviously, the insertion loss of the T/R switch is significantly important since it results in the TX efficiency reduction and RX sensitivity reduction.

Also, as the radio environment becomes more crowded, the harmonic spurious emission of the TX generates electromagnetic (EM) radiation at unintentional frequencies. The resulting pollution of the spectrum potentially desenses the radio receivers operating at the same frequency. Thus, these unintended frequency radiations must be strictly restricted, and regulatory agencies have defined some harmonic spurious emission requirements (*e.g.,* FCC 15.249). Also, the TX generates electromagnetic (EM) radiation at unintentional frequencies, and the resulting polluting of the spectrum potentially desenses the RXs operating at the same frequency. As a TX operating in the ISM band whose 2^{nd}-order harmonic distortion (HD2) locates at one of the 5G bands, the BLE TRXs must satisfy the out-of-band (OOB) spurious emission requirements (e.g., FCC 15.249). A more stringent harmonic level of BLE TRXs has been specified, which is equivalent to -41.2 dBm conducted power. As one of the key parameters of RXs, a high sensitivity performance with low power consumption is always attractive. Although the RX sensitivity is important for BLE TRXs to extend the communication distance, the strong signal handling capability (e.g., $>$ +4 dBm) is also optional for robust data links, which is expected to be demodulated with a lower RX power, particularly where the high output power devices inquiring or transmitting very close to another device. One of the major problems associated with the on-chip PA design in CMOS technology is the high loss in the power transformation and combination. This is mainly caused by the low resistance of the substrate and also the non-ideal conductor. In a typical case, the top metal is the thickest and is usually implemented for inductors or transformers. To minimize the on/off-chip area and realize high-efficiency PA, the inductors or transformers should be optimized with some process limitations.

In recent years, some BLE transceivers are proposed with significant power reduction [11, 12, 17, 81–88]. Some of them shows high-level integration with relatively small power consumption and occupied area. The co-designs of the RFIO, LNA and PA has been reported in [12, 17, 84, 86, 87, 89, 90]. However, few of them achieve both ultra-low power consumption (e.g.,$P_{\text{RX}} < 3\,\text{mW}$ with lower than -90 dBm sensitivity) and minimized on-chip area (e.g., $< 1\,\text{mm}^2$) while embedded with a T/R switch. The previous work [11] indicates the possibility of realizing an ultra-low power consumption TRX with an on-chip T/R switch while maintaining a small on-chip area by utilizing a hybrid-loop

structure.

To address the mentioned challenges, a matching network reused T/R switch with embedded TX harmonic suppression function and LNA bypass route integration is introduced. The presented BLE TRX features a direct 50 Ω single-ended antenna interface, large receiver dynamic range with corresponding power control, and ultra-low power consumption both in TX/RX mode. We detail the design and implementation of T/R switch counterpart in [14] with a detailed analysis of the proposed switch in TX and RX mode, respectively. A more detailed BLE TRX operation and measurement results are also given.

3.1 Overview of BLE Transceiver Design

Fig. 3.2 shows a block diagram of the BLE TRX. The proposed RFIO with embedded T/R switch function is integrated within a minimized on-chip area. The fully-passive suppression network in RFIO satisfies the TX OOB spurious emission requirements in the single-point direct frequency-modulation (DFM) TX. The wide-bandwidth operation of the implemented DPLL [11, 15] simplifies the TX design with lower power consumption. Since the quantization range of the high-resolution TDC (2ps) can become much narrow with the assistance from a 10 bits DTC, the total power of DPLL can be reduced significantly, and good in-band phase noise can be achieved simultaneously [91]. The wide-bandwidth also reduces the frequency settling time at the PA startup and therefore improves the TX efficiency.

To improve the input-power tolerant of the RX, the proposed RFIO provides two receiving paths of LNA enable route (high/mid gain mode) and bypass route (low gain mode), which are selectable via the SPI control codes. By properly configuring the front-end path, which corresponds to the input signal power level, a large dynamic-range (-94 dBm – +10 dBm) RX can be realized, and RX power consumption can be optimized. The noise figure degradation from the RFIO is minimized to achieve a -94 dBm sensitivity, and a close-loop DAC feedback technique in [11] is also implemented to enhance the RX dynamic range. To further lower the analog baseband's power consumption, the single-channel demodulation method [92] and a hybrid-loop RX structure based on the wide-bandwidth DPLL [11] are utilized to reduce redundant blocks. In the RX, the DPLL serves as an LO source for the mixer, and it also works as the ADC by using the VCO as the voltage to frequency (V2F) converter. Thus, the on-chip area can be further shrunk, and the power requirement can be reduced.

A compact on-chip transformer converts the RF signal to differential mode with a low-power single-input low noise amplifier (LNA), and it acts as the power combiner with HD2 termination for the differential power amplifier.

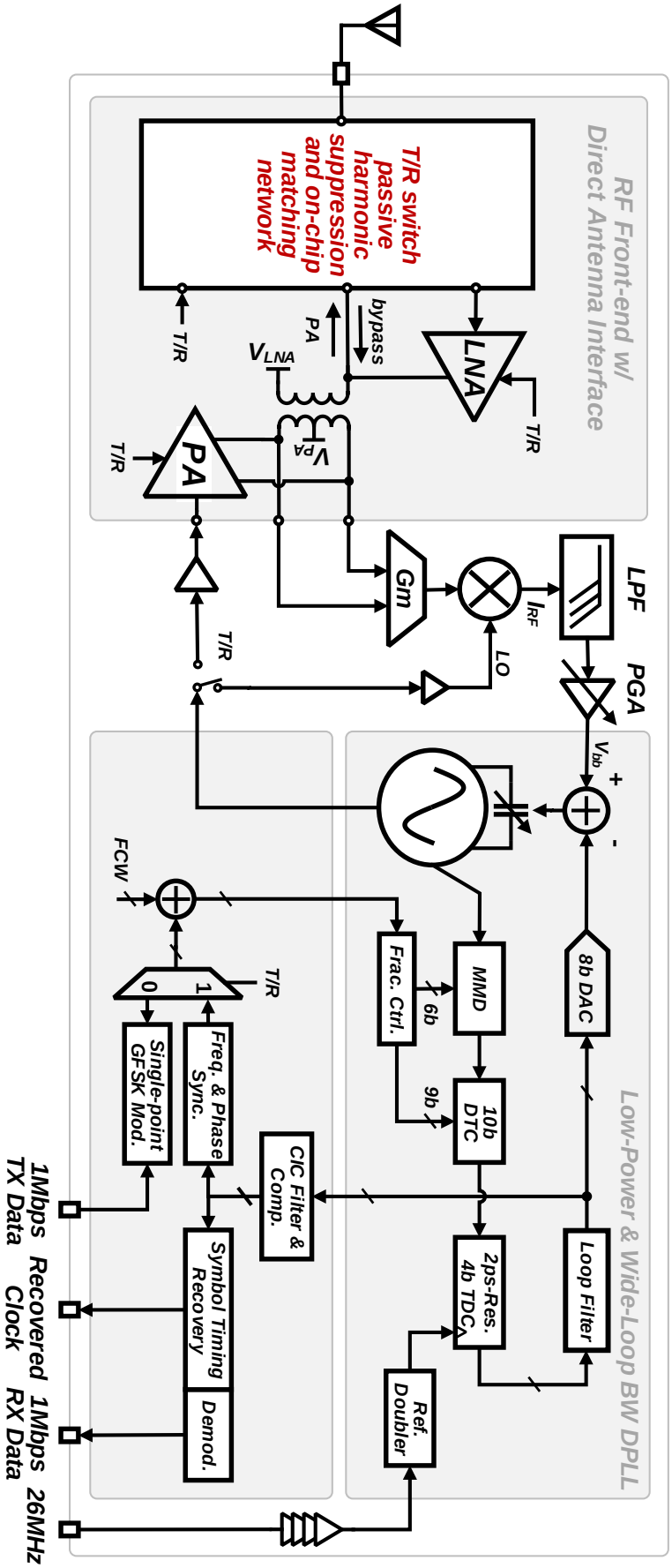


Figure 3.2: Block diagram of the proposed BLE transceiver.

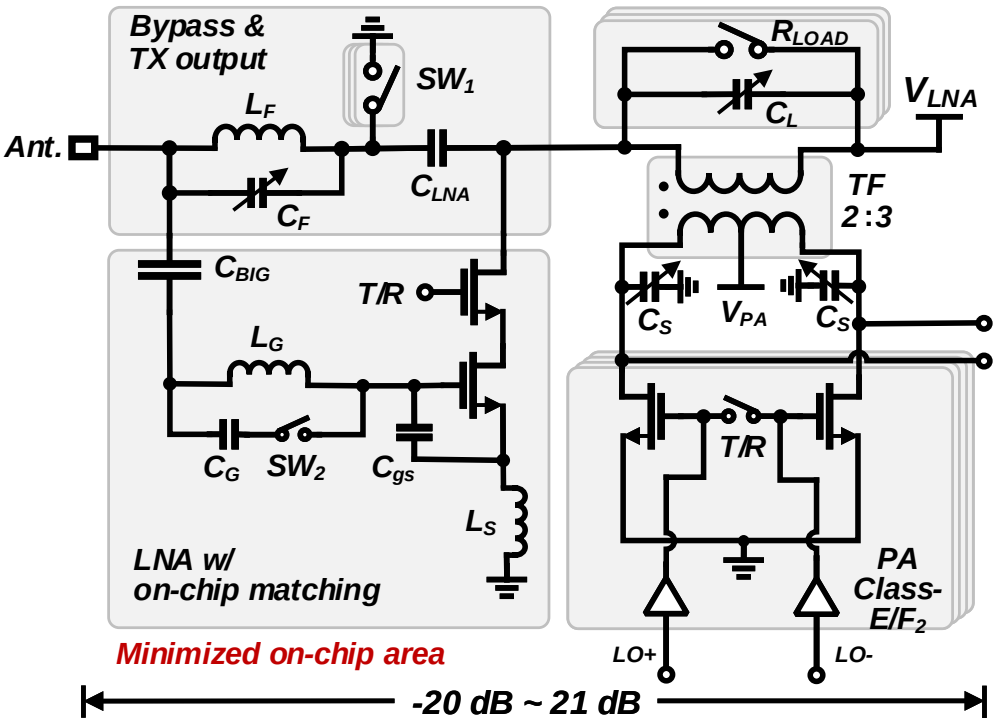


Figure 3.3: RF front-end with direct antenna interface.

This chapter is organized in the following manner. In Section 3.2, the proposed RFIO with T/R switch architecture is presented, including the details of implemented transformer. Section 3.4 and Section 3.3 discuss the BLE TRX working with the proposed RFIO in the RX mode and TX mode, respectively. Section 3.5 describes the experimental results.

3.2 Radio-Frequency Input-Output

CMOS technology scaling has provided a gratifying path toward both denser and faster integration. However, the on-chip area of passive components, mainly occupied by inductors and transformers, will maintain an area that is difficult to reduce. The RF front-end of the BLE transceiver with direct antenna interface is shown in Fig. 3.3. Through maximally reusing the passive on-chip components, including but not limited to the inductors, a harmonic-suppressed TX and high input power tolerant RX can be realized within a small on-chip area with an embedded T/R switch function.

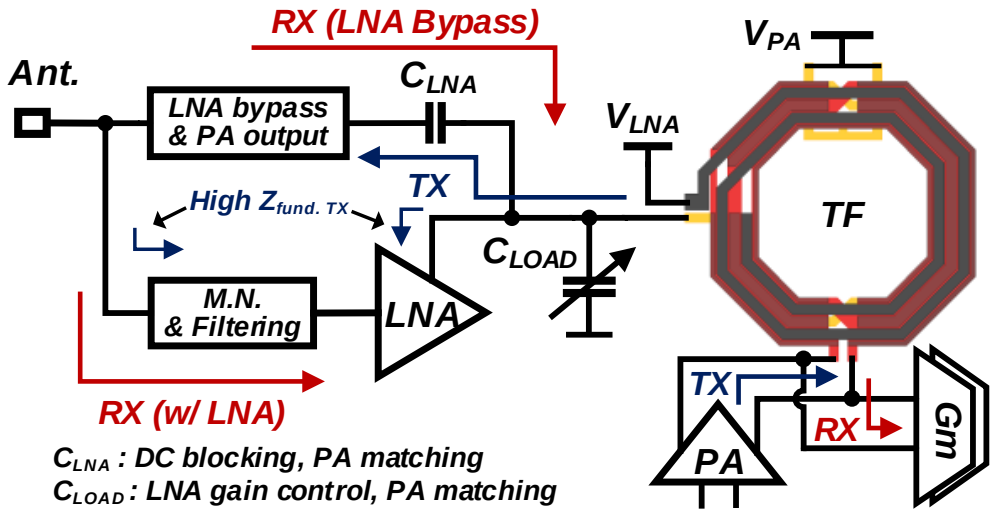


Figure 3.4: RFIO block including the LNA, LNA bypass, transimpedance amplifier (G_m) and last stage of class-E/F_2 PA.

3.2.1 RFIO

In this paper, a proposed radio-frequency input-output (RFIO) in Fig. 3.4, is embedded with an on-chip T/R switch, impedance matching, and harmonic-suppression. The proposed RFIO allows 50 Ω antenna to be connected with the single-ended RFIO pin within a miniaturized on-chip area. An RF input bypass route is also integrated to enhance the dynamic range of the receiver while sharing the same route with the PA output.

To minimize the NF degradation and power loss introduced by the conventional T/R switch integration, the size of the series transistors needs to be large, while the large parasitic capacitance degrades the NF and seldom of them achieve lower than 0.5 dB insertion loss (IL) [9]. The resonator-based switch has been introduced in [8] and the T/R switch function in this transceiver can be realized by reusing the on-chip matching inductor (L_G) and the inductor for harmonic filtering (L_F). Capacitor C_{LNA} serves as a fixed capacitance of LNA load network in the RX mode with LNA operation, and it serves as a DC blocking capacitor in LNA bypassed RX mode and cooperates with TF to block the DC and harmonic frequencies in TX mode. Note that the DC supplies of the LNA and the PA are applied at the primary windings and the center tap of the secondary, respectively. As a part of the matching network of TX, the capacitor C_L also serves as an LNA gain controller in RX mode.

Transformer-based TX matching network consisting of a transformer, C_{PA} and C_L provides high impedance for HD2. The HD2 will be further suppressed by the common-mode rejection of the TF. The resonator consisting of L_F and C_F are configured to resonate at third-order frequency to suppress the HD3, and the HD3 is further filtered by the input

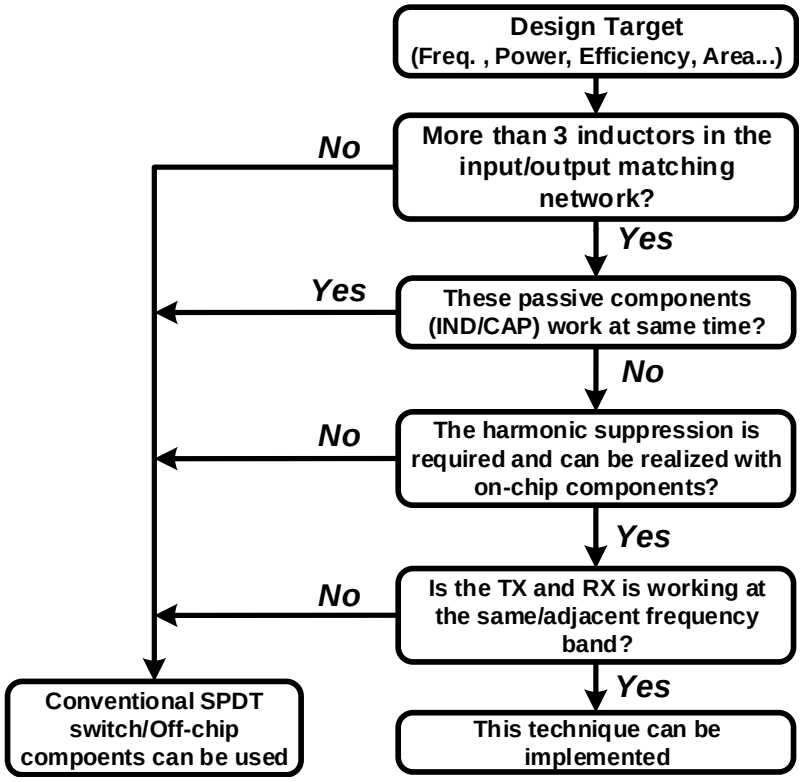


Figure 3.5: The consideration of the proposed RFIO in low-power and small-area transceiver design.

matching of LNA from its bandpass characteristic. Therefore, the TX matching network acts as an HD2 terminator, while the LNA input matching network provides more HD3 suppression. In the TX mode, the LNA transistors are turned OFF and introduce negligible TX power loss thanks to the high impedance seen from the drain node of cascode LNA. Note that the bias of G_m is OFF, therefore, only small parasitic capacitance is introduced by the gate of the G_m transistors, and it can be absorbed into the fixed part of the adjustable C_{PA}.

Design Procedures of RFIO

The proposed RFIO can be potentially implemented in low-power and small-area transceiver designs. The consideration flow of the feasibility of this structure in other designs is shown in Fig. 3.5. This technique is suitable for designs that work at time division mode with multiple inductors. Also, to switch the matching network, the frequency of both TX and RX should work at the same frequency band. Otherwise, the inductance of the input and output will be totally different, which is difficult to be shared with each other. After confirming the feasibility of these proposed techniques, there are mainly four steps to de-

signing this circuit.

Step 1: Design the cascode LNA and PA individually use the same transformer as the load inductors. The transformer design should mainly be based on PA simulation results.

Step 2: Design LNA matching network for two modes, impedance matching for RX mode and HD3 filter network (L_G, C_G, L_S). These two functions should be realized with fixed inductor value by only switching the C_G (the gate capacitance of LNA's input transistor should also be considered).

Step 3: Choose proper L_F and design C_F range to resonate at fundamental frequency to isolate the feedback of LNA and resonate at HD3 to filter the harmonic. This step should depend on the simulation results of the LNA's NF performances. The resonate impedance of L_F, and design C_F should be maximized at the fundamental frequency.

Step 4: Choose proper $R_{ON,S1}$ (depends on transistor size) and C_{LNA} to add an AC ground as part of LNA's load and PA's output matching. The value of $R_{ON,\,S1}$ is mainly determined by the required voltage gain and the stability of the LNA. While the C_{LNA} is mainly determined by the output matching of the PA side.

3.2.2 LNA and G_m

Since the RF current domain receivers, which use a low-noise trans-impedance amplifier (LNTA) followed by a passive mixer, shows superior linearity performance than a conventional LNA operating in voltage domain, the RF current domain receivers become popular in the BLE transceivers [11, 17, 88, 92]. To achieve lower power consumption, low supply voltage is commonly applied in the LNA/LNTA design [88][92]. A current-reusing structure is proposed in [11] without lowering the supply voltage. Since the conventional cascode LNA shows good enough noise performance with low power consumption and sufficient voltage gain with a robust implementation [93], a 0.6 V supply voltage cascode LNA is implemented and easily combined with the RFIO, which is followed by a transconductance amplifier (G_m), as shown in Fig. 3.6.

Instead of directly connecting the PA transistors with LNA input matching network [89], the PA transistors are connected with the secondary windings to avoid introducing low quality-factor capacitance in the gate of the input transistor, and the high voltage gain from the LNA also minimize the NF degradation caused by the introduced PA transistors.

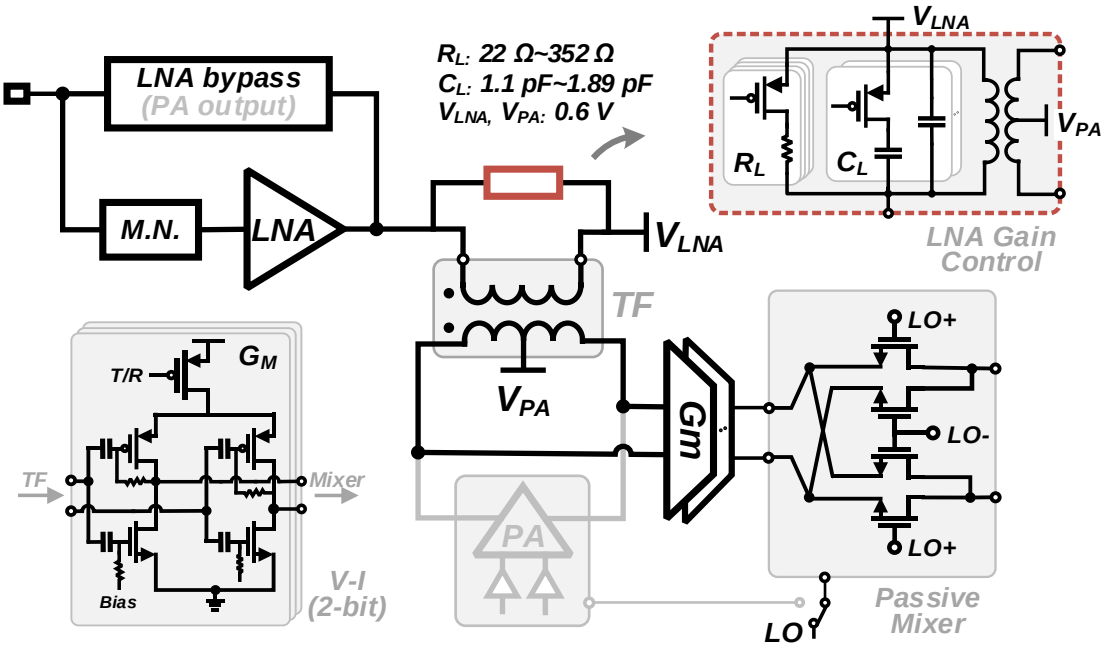


Figure 3.6: RF building blocks including LNA, G_m and passive mixer.

DC offset due to the LO leakage can also be mitigated in the high gain mode thanks to the isolation between the input of LNA and the PA transistors. Variable gain control is integrated with the LNA by adjusting the load shunt transistors.

Meanwhile, the LNA gain degradation from the PA transistors is also negligible because of the much larger resistance of the off-state PA transistors than the LNA load impedance. In order to bypass the LNA in the RX low-gain mode, both of LNA and PA transistors are turned off while the TF transfers the input signal to G_m directly. The C_G is configured to resonate with L_G at the fundamental frequency, in case of RF stress on the gate of LNA due to the large input signal. A good matching condition is maintained with appropriate on-state switch resistance (SW_1) in LNA bypass mode.

3.2.3 PA

As the most power-hungry RF component in the TX operation, the design of integrated PA is confronted with several critical problems, including high power-added efficiency (PAE) with relatively low output power and strict out-of-band spur emission. To enhance TX efficiency, switching PAs are commonly employed with efficiency theoretically approaching 100%, which also introduces strong harmonics. A class-D PA which has the lowest insertion loss theoretically is an attractive candidate for 0 dBm output power application, such as BLE [86]. However, its poor HD2 performance limits its practical application, which is from the asymmetrical switching. One-time HD2 duty cycle cali-

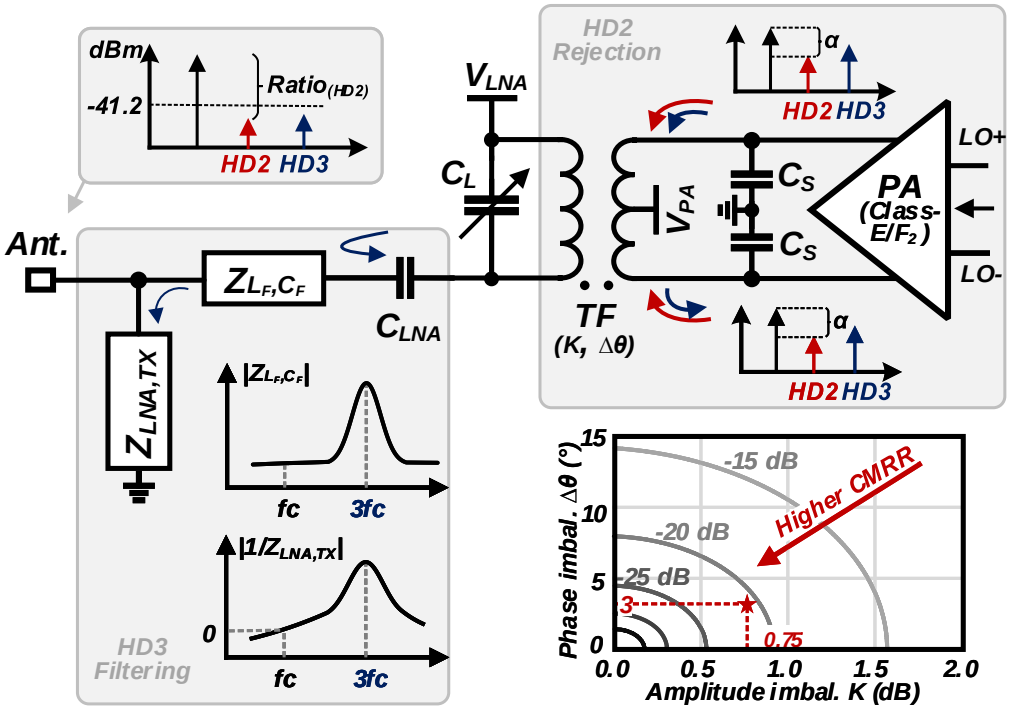


Figure 3.7: Common-mode rejection with phase and amplitude imbalance and HD3 filtering network.

bration by making the DC voltage approach the $V_{DD}/2$ is effective in suppressing its HD2 component but helpless on the odd components suppressing. Thus, the RFIO including matching network is designed with on/off-chip components to provide bandpass/notch filter for further harmonics suppression [12][86][94][95][96]. The introduced on-chip filtering network has to be considered seriously since it introduces NF degradation due to the limited impedance in RX mode. Besides that, the additional calibration loop consumes more power while the filtering network takes additional off/on-chip area, and it is contrary to the low-power consumption and miniaturization of TRX.

While considering common-mode component from the differential PA, the HD2 will experience common-mode rejection from the balanced to imbalanced port, as shown in Fig. 3.7. Since the common-mode rejection ratio (CMRR) suffers from the phase and amplitude imbalance of transformer, the HD2 emission ratio can be expressed in dB with phase and amplitude imbalance effect as

$$Ratio_{(\mathrm{HD2,dBc})} \approx 10\log_{10}(1+\mathrm{K}^2-2\mathrm{K}\cos^2\Delta\Theta)+\alpha-3 \tag{3.1}$$

Where the K and $\Delta\Theta$ are the amplitude imbalance and phase imbalance of the HD2, respectively. The α represents the power ratio in dBc between the HD2 and the fundamental frequency from PA's single branch, which mainly depends on the PA's structure

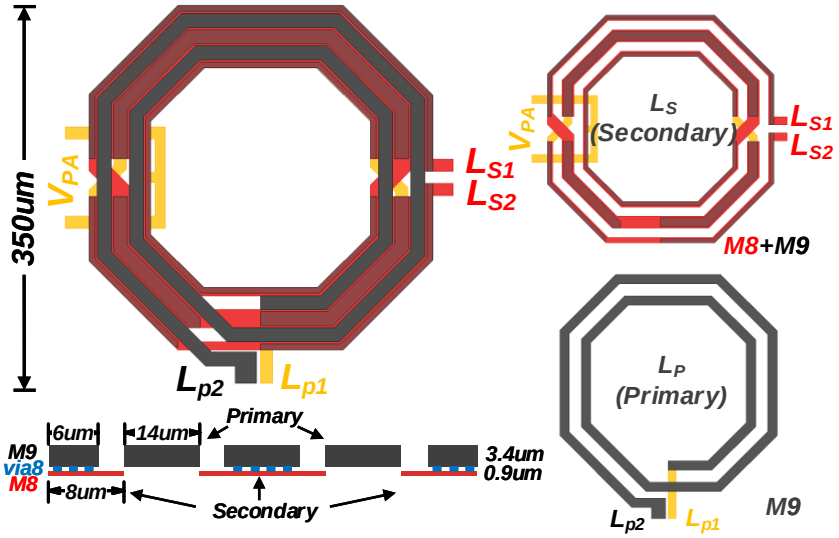


Figure 3.8: High efficiency and balanced transformer with compact area.

and matching network selectivity.The maximum HD2 emission ratio can be reached when the term of $(1+K^2-2K\cos^2\Delta\Theta)$ is close to 0. That means K and $\Delta\Theta$ should be as close as possible to unity and 0°, respectively, which are sensitive to asymmetric between transistors, besides the TF's own characteristic. The second term in (3.1) shows how the HD2 emission suffers from the single-branch PA harmonic characteristic. The stronger HD2 generated from the single branch of the PA, the more stringent requirements for K and $\Delta\Theta$ should be satisfied. Therefore, to relax the TF design and also discard the usage of the calibration circuits, a high-efficiency PA with a lower HD2 component is desired.

In this work, a switched-mode class-E/F_2 PA topology [97] with 0 dBm output power is adopted to relax the balance requirement of the transformer. Both features of efficient class-E and HD2 terminated inverse-F can be realized by using part of the RFIO and the transformer. Reusing the input matching network of the LNA, which consists of L_F, L_G and L_S to provide HD3 filtering function, the area required by TX can be further minimized.

3.2.4 Transformer

High efficiency and balanced transformer with a compact on-chip area is shown in Fig. 3.8. The implemented transformer plays different roles in TX and RX mode: (1) realizing 2^{nd}-harmonic rejection while offering the appropriate inductance for class-E/F_2 operation, (2) scaling up load impedance seen by transistors to achieve higher TX efficiency [5] and realizing power combining, (3) enabling a single-ended LNA solution and reducing the LNA power consumption compared with differential LNA structure [98]. Note that increas-

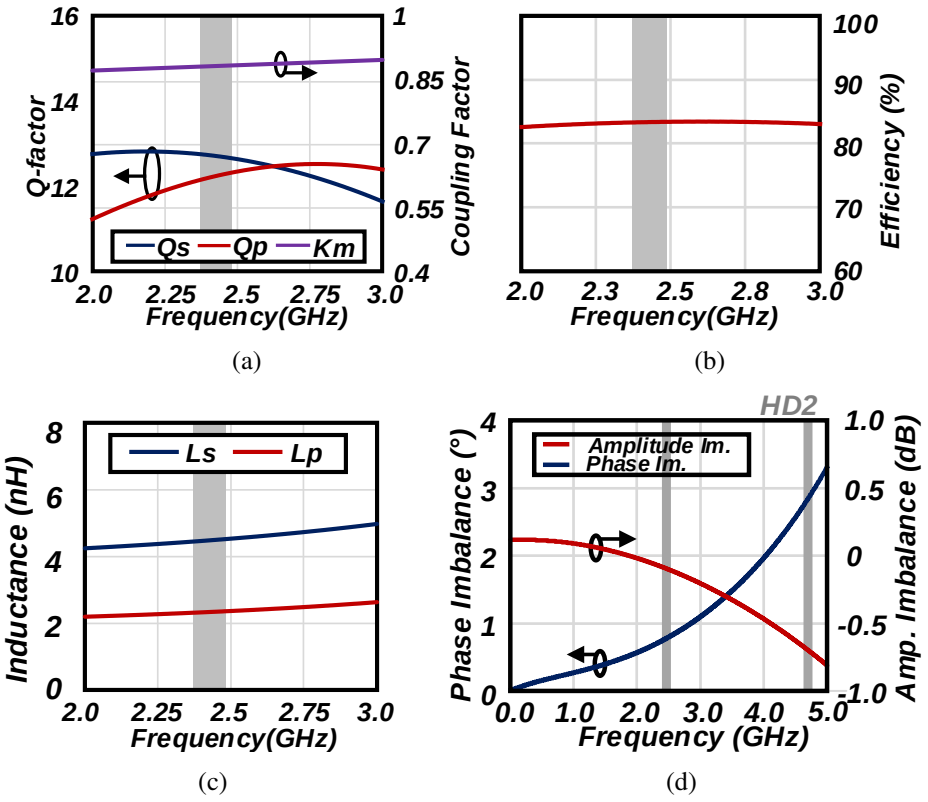


Figure 3.9: EM simulation results of the transformer: (a) Q-factor and coupling factor (b) Transformer efficiency (c) Inductance of both windings (d) Amplitude and phase imbalance.

Table 3.1: PERFORMANCES SUMMARY OF TRANSFORMER DESIGNS

	This Work (Transformer)	[99]	[17]	[100]	[101]
Technology	65nm CMOS	65nm CMOS	28nm CMOS	180nm CMOS	180nm CMOS-IPD
Frequency (GHz)	2.44	1.845	2.50	1.8	4.5
$L_{primary}$ (nH)	2.3	2.82	0.43	1.89	N.A.
$L_{secondary}$ (nH)	4.5	7.46	1.41	5.07	N.A.
$Q_{primary}$	12.2	4.84	11.4	7.31	N.A.
$Q_{secondary}$	12.7	6.12	16.8	9.99	N.A.
k_m	0.88	0.94	0.76	0.72	N.A.
Efficiency ($\eta_{p,\,maximum}$)	83.4%*	67.8%	82.7%	72.3%	N.A.
Efficiency ($\eta_{p,\,R_L=50\Omega}$)	81.8%*	64.7%	46.5%	58.3%	83%

* calculated based on simulation results and equations from [44].

ing LNA gain without additional power overhead and scaling up the antenna impedance for low-power output impedance matching can be achieved simultaneously with a step-up transformer ($L_{P,S}$) structure. As the central component of the RFIO, the transformer needs to be optimized in multiple aspects, including the adequate impedance transformation in TX mode and available loading impedance in RX mode. The imbalance performance, including phase imbalance and amplitude imbalance, should also be minimized for TX-HD2 termination and RX common-mode noise rejection.

$$\eta = \frac{1}{\frac{2}{Q_P Q_S k_m^2}(\sqrt{Q_P Q_S k_m^2 + 1} + 1) + 1} \tag{3.2}$$

As illustrated in the [44], the power combination efficiency η can be maximized using a coupling factor k_m as close as possible to unity, which is intuitively reflected in the equation (3.2), where Q_P and Q_S represent the Q-factors of the primary and secondary windings of the transformer, respectively.

Typically, only one ultra-thick metal, copper (*Cu*), is available in the back end of the line (BEOL) in digital-oriented CMOS. To maximum utilize the presence of the one thick *Cu*, the on-chip transformers are usually built up in a co-planar structure and coupled with each winding [17]. To achieve a higher Q-factor, the single-turn windings and co-planar structure are implemented in [17]. To mitigate the on-chip area, the vertical layout integration with pattern ground shield (PGS) is also adopted by making the active devices under the transformer, which inevitably raises the layout difficulty. To minimize the on-chip area as much as possible while maximizing the coupling factor k_m, a stacked transformer with

one thick *Cu* primary winding and one aluminum *Al* secondary winding has been presented in [99]. In order to minimize the on-chip area and achieve suitable inductance, the 2 : 3 turn transformer with only one ultra-thick metal (UTM) layer is implemented, which occupies the same area as a single inductor. The compact on-chip area, the high Q-factors of both windings, and also the higher coupling factor. All these are desired with only one available thick *Cu*. In this CMOS technology used in the prototype, only one ultra-thick metal (UTM) layer is available, which has a thickness of over 3 μm. The primary winding is implemented using the single UTM M9, with one thin lower metal being used as port connection L_{P1} for LNA. Meanwhile, the port L_{P2} in M9 can be directly connected to the LNA's supply voltage (V_{LNA}). The inner radius and metal width are optimized to provide appreciate inductance and a high Q-factor. Fig. 3.8 introduces a high k_m transformer, with highly balanced performance using only one ultra-thick metal (UTM). Instead of implementing the stacked transformer structure [99], the secondary winding is constructed with both the upper *Cu* metal M8 and UTM M9 to minimize parasitic resistance while the width of the inner and outer ring can be reduced to 6 μm. An odd number of turns in secondary windings provide a symmetric structure whose crossovers are equal. A 90° rotation is applied on the secondary winding, allowing only M7 and M8 as crossovers for the primary winding, and also facilitate the layout distribution by changing the signal direction, simultaneously. The electromagnetic (EM) simulation results are given in Fig. 3.9. With the assistance of an additional metal layer M8, our transformer achieves both of the windings' Q-factor over 12, and the coupling factor k_m between two windings over 0.88 at the operation frequency of interest, as shown in Fig. 3.9(a). The value of $Q_P Q_S k_m^2$ in the ISM band proves more than 83% maximum efficiency is available, as shown in the Fig. 3.9(b).

As described in the Section 3, to achieve lower than -41 dBc HD2 suppression level with 0 dBm fundamental power, the total phase and amplitude imbalance can be relaxed to 20° and 2.7 dB in case of $\alpha \leq 14$ dBc, respectively. In the EM simulation, lower than 3° phase imbalance and 0.75 dB amplitude imbalance are available from the implemented TF while relaxing the HD2 suppression in the TX mode without occupying the additional area. This multi-layer transformer shows both high coupling and Q-factors and good imbalance performances, which demonstrate its practicality as the central part in this RFIO design.

3.3 High Dynamic-Range Low-Power Receiver

Some ISM-band receivers are presented with high sensitivity [11, 12, 17, 81–84, 86–88, 92, 102–105] while mixer-first RXs show much lower power consumption [84, 103].

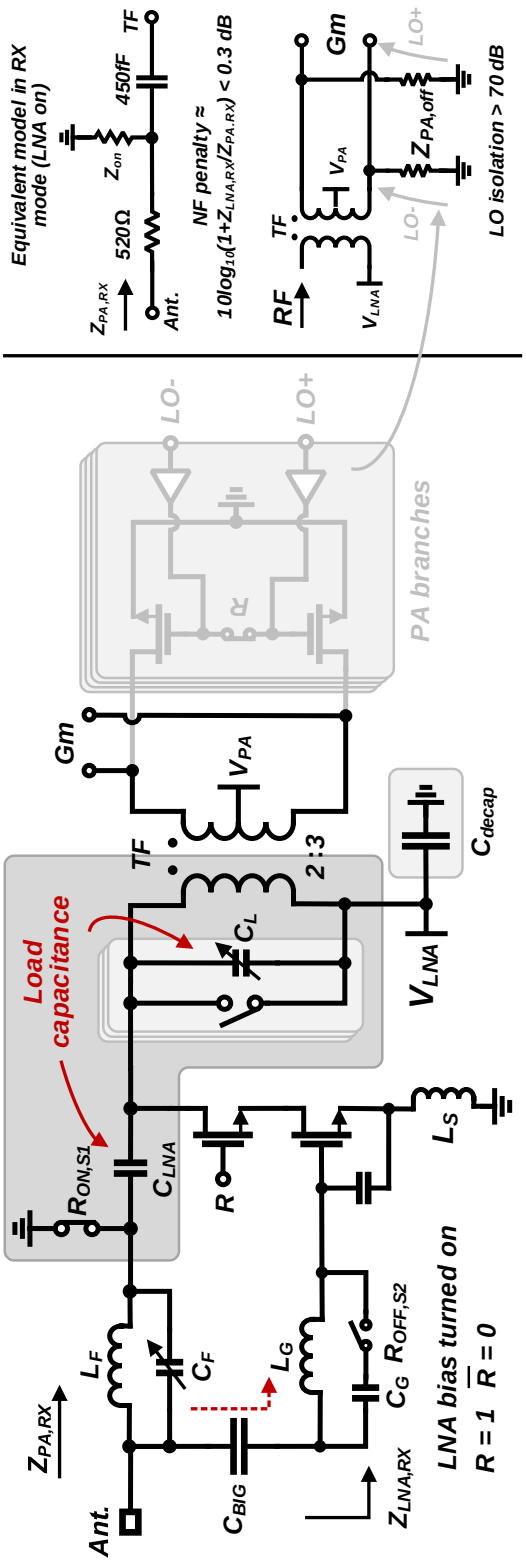


Figure 3.10: BLE transceiver in RX high/mid gain mode.

Since high power transmission in practical applications where short ranges could be encountered may cause the RX to be saturated. Even though the received power control requests shall be supported with power class 1 Bluetooth devices, the enlargement of the RX input power tolerance ($>+4$ dBm) is also an alternative way to ensure the fast and reliable link. Also, the power consumption of the receiver can be optimized to extend its life-time according to the input signal strength and application scenarios. Since the LNA bypass route can relax the linearity of the front-end while the RX power can also be reduced. Meanwhile, the high RX sensitivity requires a low noise factor. Thus, minimized noise factor penalty and high input-power tolerance through configuring the RX input network are desired in the implementation of RFIO within an identical on-chip area.

With the emergence of new Bluetooth standard (v5.1) [4], the communication distance is enhanced with several times compared with the BLE (v4.2), using a maximum of 20 dBm output power (maximum output power for LE in v4.2 is 10 mW), when communication between different distances exists at the same time Some BLE receivers are proposed with significant power reduction while achieving high sensitivity [11, 12, 17, 86, 88, 92]. As two of the most popular RX structures for frequency-shift keying (FSK) systems, low-IF, and zero-IF receiver architecture show excellent sensitivity and blocker performance by utilizing both I and Q channels [17, 86, 88], aggravating the power consumption of LO buffers and analog baseband (ABB). As another popular structure in low-power design, the sliding-IF structure with lower power required by the LO generation can achieve high power efficiency [12][83][85], although it causes image problems. In recent year, the single-path down-conversion method has been introduced in a hybrid-loop receiver [92] and consummated in [11]. The DPLL used as the LO digitizes the analog baseband signal V_{bb} through a varactor which performs as a voltage-to-frequency converter.

Phase noise requirement in ultra-low-power FSK transceivers has been analyzed in [106]. Considering the desired signal level with -67 dBm under a -40 dBm blocker at 3-MHz offset, a LO noise performance of less than -99 dBc/Hz at 3-MHz offset with lower than -40 dBc spur level is strictly required.

$$\mathcal{L}_{\mathrm{PN,max}} \approx S_{\mathrm{des}} - S_{\mathrm{blo}} - SNR_{\mathrm{min}} - 10\log BW_{\mathrm{eff,noise}} \tag{3.3}$$

For BLE receivers, the worst blocker case (S_{blo}) is -40 dBm specified for offsets greater than 3 MHz. While the effective noise bandwidth $BW_{\mathrm{eff,noise}}$ is increased by 250 kHz due to the noise folding from the image part [92], the phase noise floor $\mathcal{L}_{\mathrm{PN,max}}$ works out to -96 dBc/Hz for a BLE receiver requiring a SNR_{min} ratio of 10 dB to achieve lower than 0.1% BER performance. Hence, to reach a minimum sensitivity of -94 dBm

Table 3.2: LNA SIMULATION RESULT SUMMARY

	S11 (dB)	Gain (dB)	NF (dB)
LNA Only	-13.1	21.2	3.35
LNA w/ C_G	-13.6	21.1	3.46
LNA w/ C_G, L_F, C_F	-10.3	21.0	3.83
Entire LNA (w/ C_G, L_F, C_F, PA Tr.)	-10.4	21.0	3.84

and standard-compliant blocker performances, an in-band PN lower than -110 dBc/Hz low-power fractional-N DPLL is implemented with sufficient margin.

3.3.1 BLE Receiver in High/Mid Gain Mode

To realize a high sensitivity and low-power consumption receiver, the LNA is the most critical component, while hard limitation exists between the power, noise performance, and linearity. The additional T/R switch inevitably degrades the noise performance, which should be minimized.

In Fig. 3.10, the configuration of receiver high/mid gain mode is shown. As the most power-hungry part in the front-end, the single-ended input LNA with a single-to-differential load structure is designed to minimize the power consumption and reduce susceptibility to supply noise. The C_G is disconnected with the gate inductance L_G, while the shunt switch S2 is turned off with a high off-resistance $R_{ON,S2}$. In this mode, the C_{LNA} acts as a fixed part of the load capacitance in series with a low resistance value of $R_{ON,S1}$. In order to mitigate the side effect introduced by the TX output path, e.g., NF, return loss, and gain, the $Z_{PA,RX}$ are desired with high impedance and low noise contribution. A high impedance of $Z_{PA,RX}$ has three effects: 1) isolate the amplified output signal from the input port in case of instability leading by the drain-gate feedback, 2) minimize the degradation of LNA matching status due to the $Z_{PA,RX}$, and 3) reduce the input insertion loss introduced by the PA output path. Overall, the NF degradation from the TX output path should be minimized while a large magnitude $|Z_{PA,RX}|$ is desired. The resonant frequency of the parallel connection of L_F and C_F is adjusted to the operating frequency ω_0. In the operating frequency, a 520 Ω of $|Z_{PA,RX}|$ can be provided by the parallel connection of the L_F and C_F. To eliminate the influence from the TX output path on the matching status, the following equation can be utilized when the shunt switch's resistance ($R_{ON,S1}$) is ignored.

$$Z_{RX} = Z_{LNA,RX} \parallel Z_{PA,RX} \tag{3.4}$$

The total input impedance Z_{RX} seen by the antenna in RX mode can be estimated

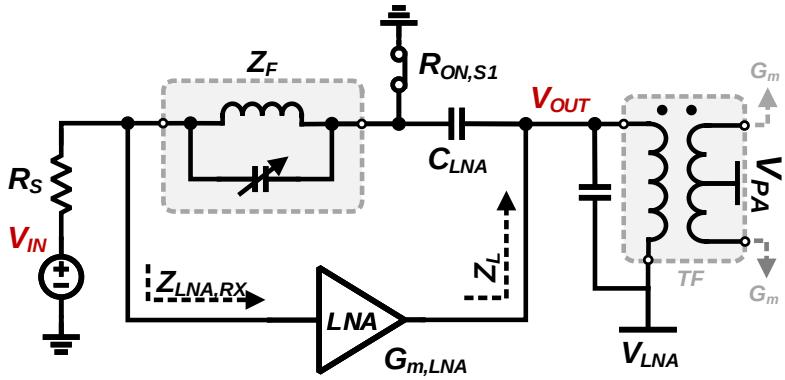


Figure 3.11: Simplified LNA model with proposed RFIO.

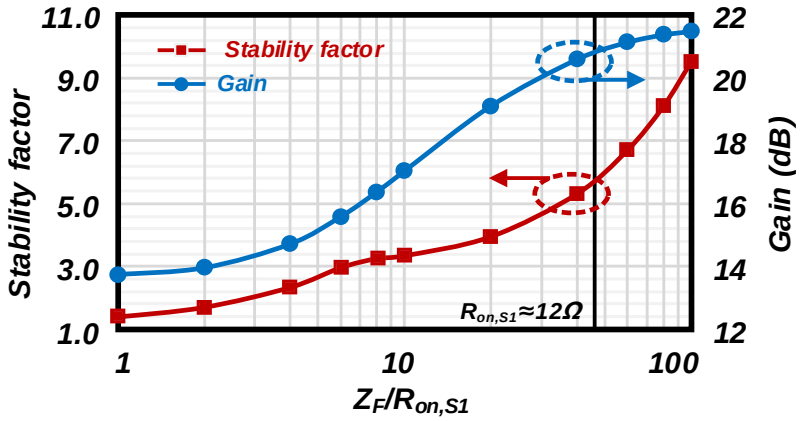


Figure 3.12: LNA voltage gain and stability factor as the function of $Z_F/R_{ON,S1}$.

by considering the parallel combination of a 520 Ω of $|Z_{PA,RX}|$ and the input impedance ($Z_{LNA,RX} \approx 37 - 5j$) from an inductive-degenerated cascode LNA [107]. The return loss can be as low as -15.9 dB without obvious degradation in post-layout simulation, compared with no T/R switch case, thanks to the comparatively high impedance from the $Z_{PA,RX}$. The NF degradation is minimized to 0.5 dB while maintaining a good matching condition.

Fig. 3.11 simplifies the operation of the LNA with proposed RFIO in RX high/mid gain mode. The V_{IN} represents the input signal from the antenna port. Amplified signal V_{OUT} is generated with LNA transconductance gain $G_{m,LNA}$ and load impedance Z_L provided by TF with capacitance including C_{LNA}. As shown in the LNA high/mid gain mode in Fig. 3.11, one feedback loop is presented between the V_{OUT} and V_{IN}. We have

$$\frac{V_{OUT}}{V_{IN}} \approx g_{m,LNA} Z_L \frac{1 + \frac{Z_F}{R_{ON,S1}} + sZ_F C_{LNA}}{1 + \frac{Z_F}{R_{ON,S1}} + sC_{LNA}(Z_F - R_S g_{m,LNA} Z_L)} \tag{3.5}$$

Fig. 3.12 plots the LNA voltage gain and stability factor versus the $Z_F/R_{ON,S1}$. With the assistant of NMOS switch transistor (S1) which has a on-resistance $R_{ON,S1}$ range from 12 Ω to 46 Ω, a maximum 21 dB LNA voltage gain can be obtained with a $Z_F/R_{ON,S1} \approx 43$ while sufficient stability factor (>5) is also achieved.

The total power consumption of the LNA and Gm can be reduced to 0.7 mW, while a 0.6 V supply voltage is applied on the LNA. With fully on-chip impedance matching, the minimum noise figure of the LNA with the embedded T/R switch is 3.84 dB. The total RX front-end achieves 6.5 dB minimum noise figure integrated with 1-MHz bandwidth, using the spectrum analysis method shown in [108]. A 250 kHz IF is adopted, which enables the conversion of GFSK to DBPSK and demodulation only with a single channel. A current-driven double-balanced passive mixer is implemented to avoid introducing additional flicker noise and power overhead while providing higher linearity compared with active mixer [109]. The low-pass input impedance of the analog baseband transimpedance amplifier (TIA) is frequency transferred by the passive mixer to the output of the Gm [110][111]. The filtering bandwidth is approximately 750 kHz which is sufficient for a 1-MHz demodulated baseband signal. The maximum PGA gain is 28 dB with 7 dB gain steps. By using only I-channel for demodulation, the ABB saves the on-chip area and power consumption while achieving a compromise between noise and linearity performances.

The input-referred third-order intercept point (IIP3), as one of the index of the receiver linearity, can be expressed as:

$$\frac{1}{IIP3_{\mathrm{RX}}} \approx \frac{1}{IIP3_{\mathrm{LNA}}} + \frac{G_{\mathrm{LNA}}}{IIP3_{\mathrm{Gm}}} + \frac{G_{\mathrm{LNA}}G_{\mathrm{Gm}}}{IIP3_{\mathrm{MIX}}} + \frac{G_{\mathrm{LNA}}G_{\mathrm{Gm}}G_{\mathrm{MIX}}}{IIP3_{\mathrm{ABB}}} \tag{3.6}$$

Where the $\mathrm{IIP3_{ABB}}$ represents the IIP3 of the analog baseband circuit, including the LPF and VGA.

Fig. 3.13 shows the IIP3 measurement results using a two-tone test from an oscilloscope with spectrum analysis function. In order to achieve a wanted SNR performance, the nonlinear product from in-band/out-of-band interferences should be smaller than the noise floor with sufficient margin. The in-band IIP3 of the front-end is measured using one input at 2.43450 GHz and the other input at 2.43451 GHz with an LO frequency of 2.434 GHz, which generates an in-band IM3 product at 490 kHz. The measured in-band IIP3 of RX is -56.1/-30.5/-0.1/17.5 dBm in the high/medium/low/bypass gain settings. By feeding two tones at 2.5000 GHz and 2.56551 GHz, an out-of-band (OOB) IM3 product at 490 kHz IF with a 0 dBm OOB-IIP3 can be measured with a 2.434 GHz LO.

In the case of the ABB saturated by the DC offset due to the LO self-mixing in high gain mode, a shunt switch is inserted between the gate of the disabled PA transistors.

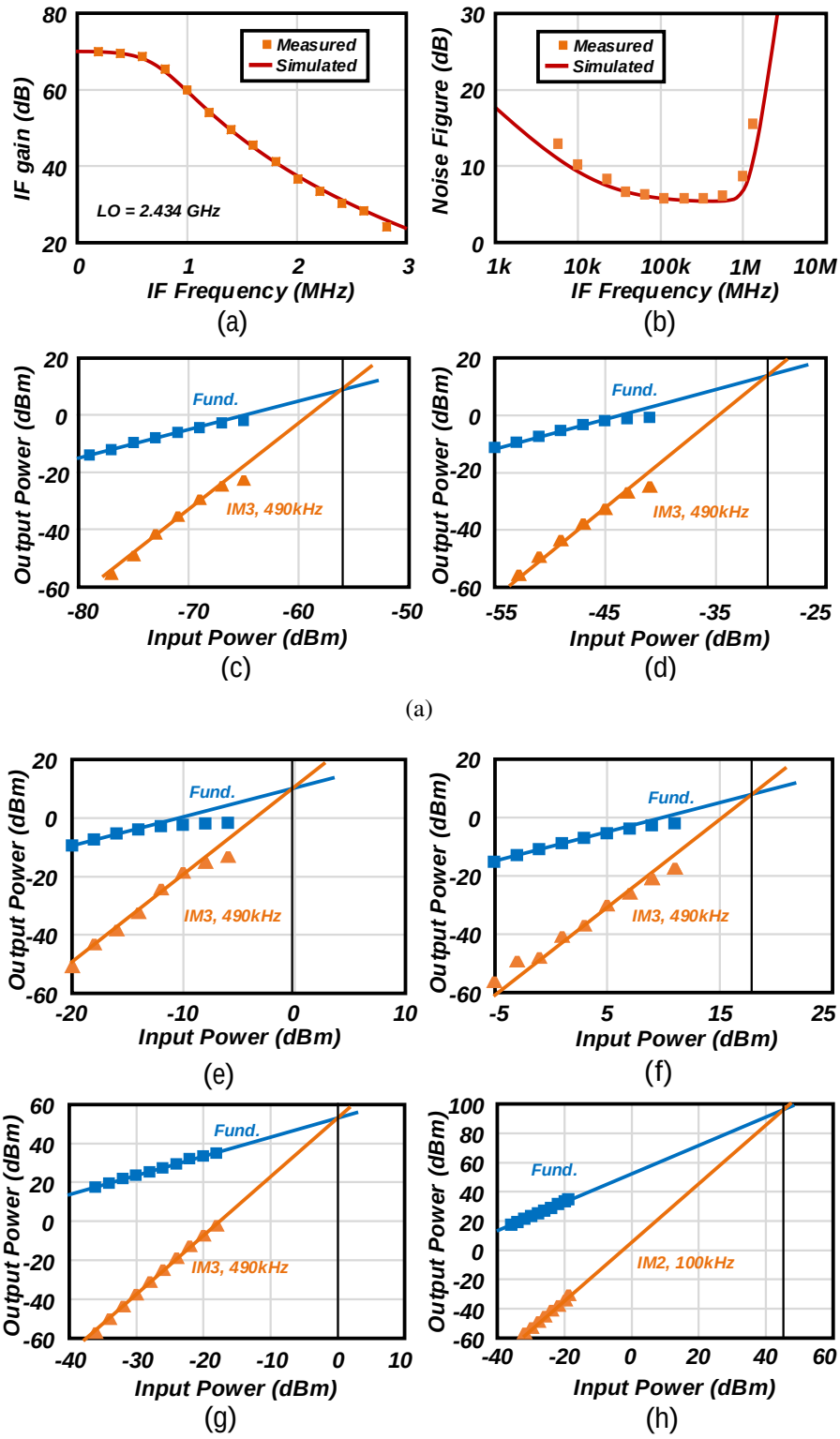


Figure 3.13: RX measurement summary: (a) maximum RX front-end gain (b) minimum noise figure of the RX (c) in-band IIP3 in high gain mode (d) in-band IIP3 in medium gain mode (e) in-band IIP3 in low gain mode (f) in-band IIP3 in bypass (negative gain) mode (g) out-of-band IIP3 (h) out-of-band IIP2.

In the post-layout simulation, the LO isolation between both ends of PA is over 70 dB, which should also thank the gated LO buffer. Since the LO leakage doesn't experience the amplification of the input LNA, the DC offset can be mitigated. To prevent the LO leakage from the substrate and radio emission, the layout of the DCO and the front-end are physically separated as much as possible, which slightly increases the required area, and the LO distribution is through the ground shielded transmission lines. A 100 kHz IM2 product is measured by using two OOB signals, one at 2.5000 GHz and the other at 2.5001 GHz. A 45 dBm OOB-IIP2 is achieved in this condition.

3.3.2 BLE Receiver in LNA Bypass Mode

To increase the front-end linearity, the LNAs typically have several gain modes. An input signal bypass is shown in the low-gain operation of a receiver only design [112]. The LNA input-output terminals are shorted by adding shunt transistors in a common way. As indicated in the [92], an attenuator at the input is implemented to attenuate the input signal in the mid/low gain mode, in which a high-Q external matching inductor is also included for better performances.

The close-loop DAC feedback technique illustrated in the [11] evidently enhances the dynamic range of the RX by preventing the voltage-to-frequency (V2F) component from working in the nonlinear region. However, the front-end still suffers from the large input power, and it is inevitable to increase the power consumption to maintain the linearity. Meanwhile, with larger than -5 dBFS input amplitude, the SNDR of the DPLL-based ADC rapidly drops as one of the measurement results shown in [11]. Thus, the bypass mode must provide sufficient attenuation (e.g., $P_{\text{in}} > +4$ dBm) in case of degrading the DPLL-based ADC performance. To mitigate the use of the off-chip components and enlarge the adjustable gain range of the front-end to maintain good linearity with large input power, the implemented front-end, which presented in Fig. 3.3 can be configured into LNA bypassed mode by using the proposed miniaturized RFIO. Therefore, a high dynamic-range RX (-94 dBm $\sim$ +10 dBm) can be realized in this BLE TRX.

While the LNA is bypassed, the trans-impedance amplifier Gm will become the first input stage. Regardless of the nonlinearity from the switch transistors, the IIP3 of the LNA bypassed mode can be expressed as:

$$\frac{1}{IIP3_{\text{RX}}} = G_{\text{RFIO}}\left(\frac{1}{IIP3_{\text{Gm}}} + G_{\text{Gm}}\left(\frac{1}{IIP3_{\text{MIX}}} + \frac{G_{\text{MIX}}}{IIP3_{\text{ABB}}}\right)\right) \tag{3.7}$$

Where the G_{RFIO} is the gain from the RFIO network, and it can be described as an attenuation in the negative case.

In this proposed BLE TRX, the LNA can be bypassed by reusing the PA output path

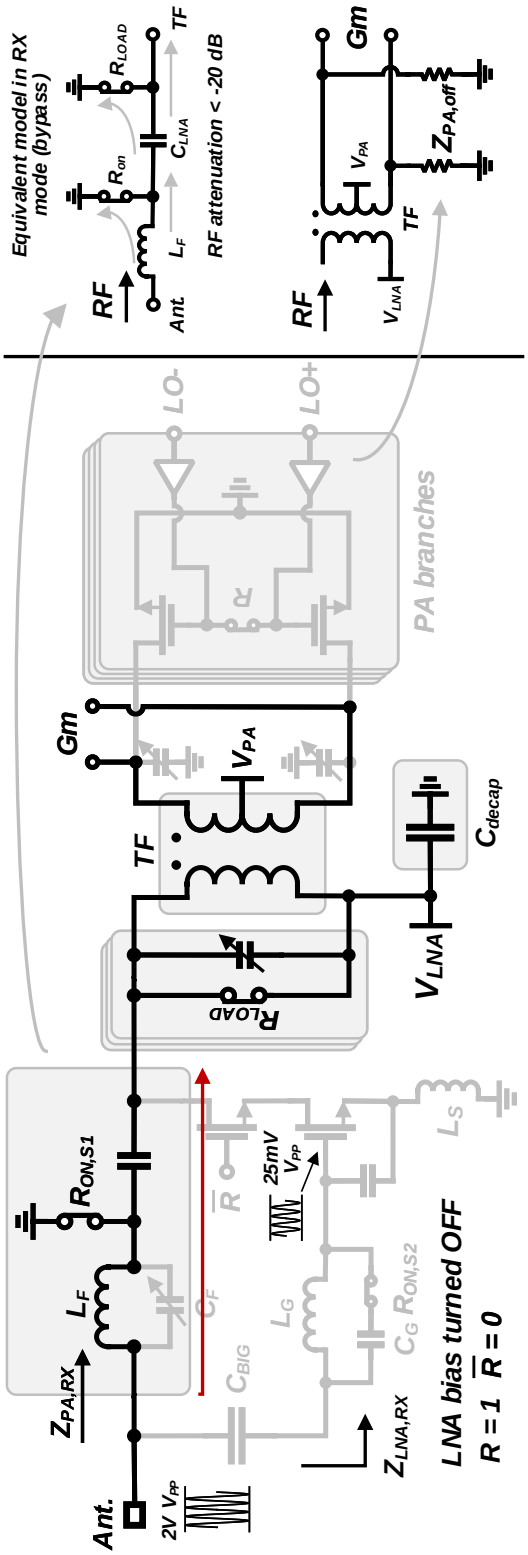
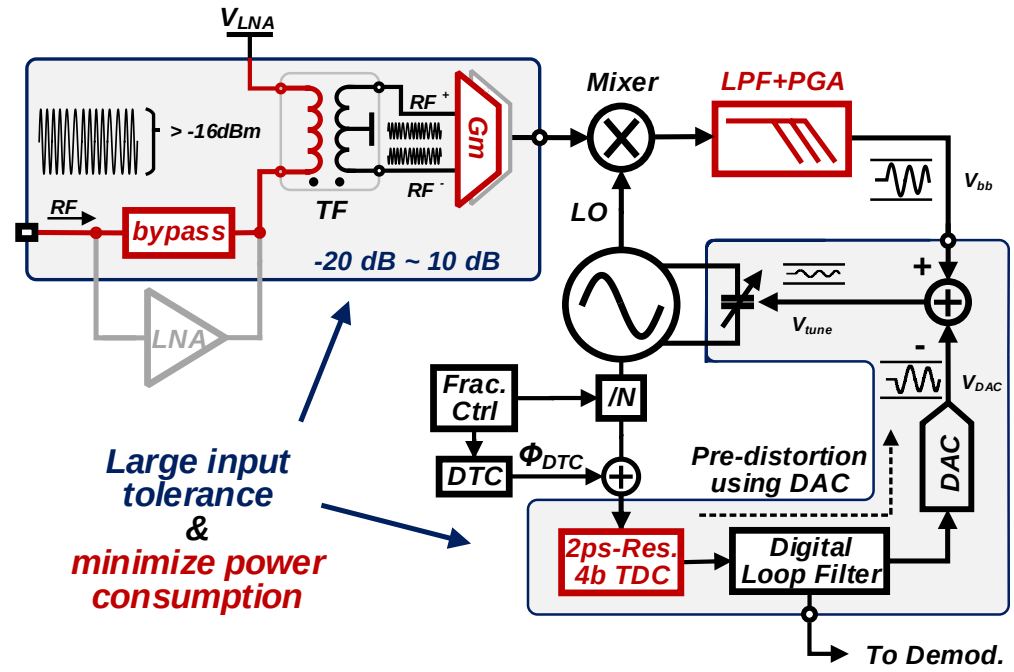
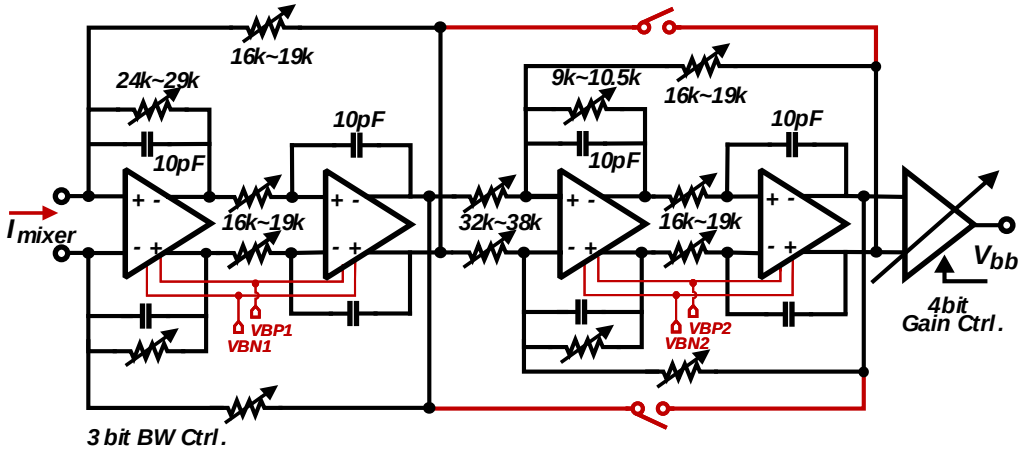


Figure 3.14: BLE transceiver in bypass (low gain) mode.



(a)



(b)

Figure 3.15: (a) Large input power tolerant RX with LNA bypass route. (b) A adjustable fully differential butterworth low-pass filter.

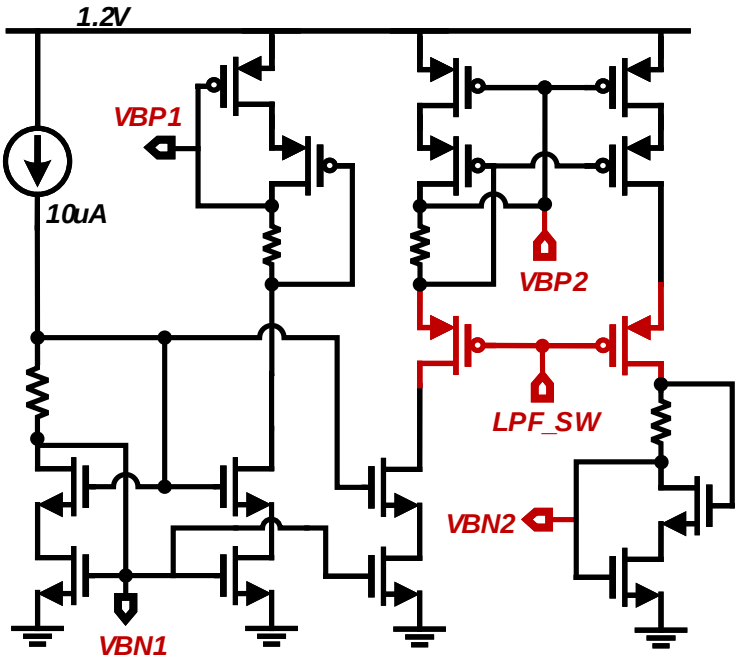


Figure 3.16: Switchable cascode complementary bias circuit for LPF and PGA.

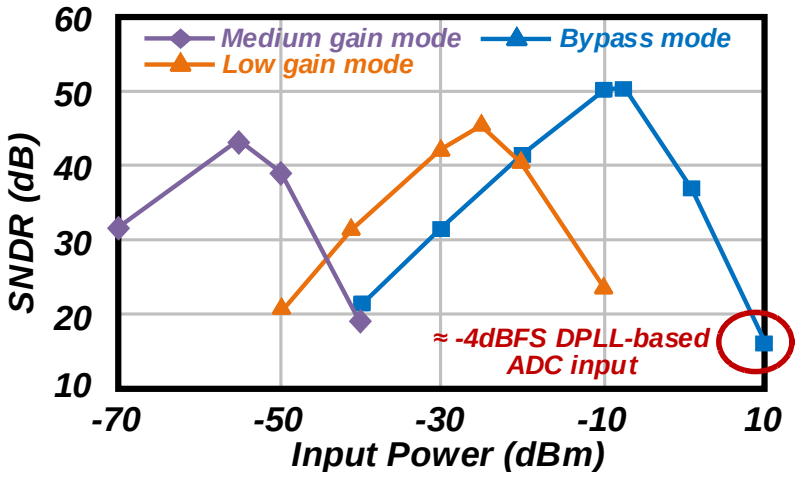


Figure 3.17: Measured result of the SNDR of the front-end from the PGA output monitor.

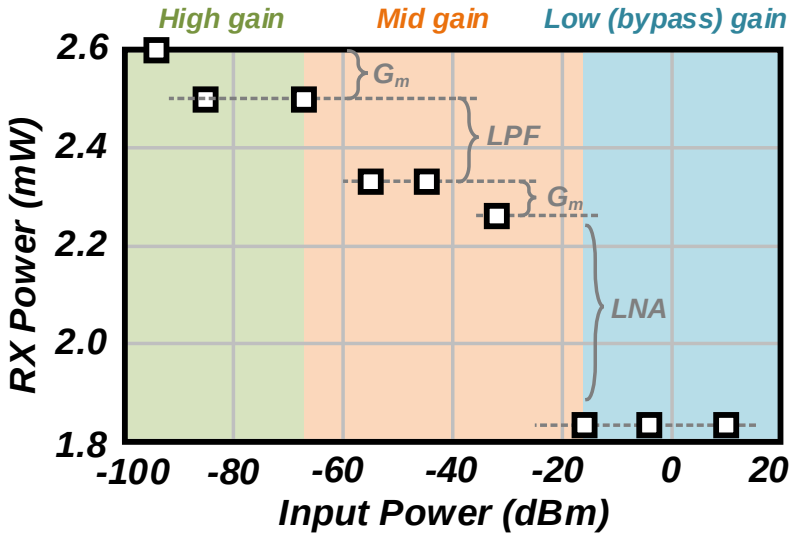


Figure 3.18: RX power consumption and gain settling with different input power.

while both biases of the LNA and PA transistors are set to low. The configuration is shown in Fig. 3.14. By tuning the capacitor C_F to the minimum value and turn on the shunt transistors to the state-on; the on-state transistors provide a low impedance R_{LOAD} for the input power dissipation, while the transformer converts the single-ended input signal to differential signals. With four independent Gm cells, which are also set to low-gain mode, this attenuated RF signal will be transferred into the current domain.

The attenuation (G_{RFIO}) of input RF signal through this bypass route can be estimated by using the following equation, while considering the on-state resistance of the shunt transistor $R_{ON,S1}$ and the impedance from the L_F, C_{LNA} and R_{LOAD}.

$$G_{RFIO} \approx -20\log\left(\left|\frac{sL_F}{R_{LOAD}} + \frac{1+\frac{sL_F}{R_{ON,S1}}}{sC_{LNA}R_{LOAD}}\right|\right) \tag{3.8}$$

By considering $L_F = 2.95\,nH, C_{LNA} = 450\,fF, R_{ON,S1} \approx 46\,\Omega$ and $R_{LOAD} \approx 22\,\Omega$, the attenuation of the RF through bypass route can exceed 20 dB. Similar to the LNA high/mid operation mode, this attenuation can be set by a thermometer-code word $R_L[3:0]$ to values in steps of 4 dB. The main concept of the power optimization and the input-power tolerant enhancement are present in Fig. 3.15. Fig. 3.17 shows the measured SNDR from the PGA output monitor. According to the input power strength and application scenarios, the RX power consumption can also be optimized. Fig. 3.18 shows the RX power consumption versus the input power. With a proper front-end configuration, the total RX power can achieve lower than 2 mW with a larger than -16 dBm input power.

The input impedance matching can still be realized in the bypass mode, which is benefit from reusing the on-state resistance of the shunt transistor $R_{ON,S1}$. While the input

impedance of the bypass mode in Fig. 3.14 can be calculated by the following equation.

$$Z_{\mathrm{BYPASS,RX}} = Z_{\mathrm{PA,RX}} \parallel Z_{\mathrm{LNA,RX}} \tag{3.9}$$

In case of the input impedance of LNA, $Z_{\mathrm{LNA,RX}}$, affecting the $Z_{\mathrm{BYPASS,RX}}$, it is desired that the input impedance mainly comes from the $Z_{\mathrm{PA,RX}}$. Hence, the $Z_{\mathrm{LNA,RX}}$ should show a high impedance at operation frequency, seen from the input port. In this condition, the main resonant frequency of the parallel connection of L_{G} and C_{G} is roughly adjusted to the operation frequency ω_0, which is similar in the TX mode. Considering the $R_{\mathrm{LNA,RX}} \gg |Z_{\mathrm{PA,RX}}|$, the $Z_{\mathrm{BYPASS,RX}}$ can be consequently estimated as

$$\begin{aligned} Z_{\mathrm{BYPASS,RX}} &\approx \left(\left(\frac{1}{sC_{\mathrm{LNA}}} \parallel R_{\mathrm{ON,S1}}\right) + sL_{\mathrm{F}}\right) \\ &= \frac{R_{\mathrm{ON,S1}}}{1+\omega^2 R_{\mathrm{ON,S1}}^2 C_{\mathrm{LNA}}^2} + s\left(L_{\mathrm{F}} - \frac{R_{\mathrm{ON,S1}} C_{\mathrm{LNA}}}{1+\omega^2 R_{\mathrm{ON,S1}}^2 C_{\mathrm{LNA}}^2}\right) \end{aligned} \tag{3.10}$$

With the parameters mentioned before, the input impedance of bypass mode, $Z_{\mathrm{BYPASS,RX}}$, can be calculated at operating frequency ($\approx 42 + 29\,j$), which also guarantees lower than-10 dB return loss in bypass mode.

The degradation of CMOS transistors under RF stress has been reported in [113][114]. Gate-oxide breakdown is catastrophic in the RF circuits and must be avoided under all situations. In case of a large RX input signal, e.g., 2 V V_{pp}, the presenting of large voltage waveform at the LNA input transistor's gate (V_{gs}) should be avoided. With the proposed RFIO, the voltage amplitude of V_{gs} can be minimized, e.g., 25 mV V_{pp}, thanks to the high resistance $R_{\mathrm{LNA,RX}}$ ($\approx 1.3\,\mathrm{k\Omega}$) introduced by the parallel connection of L_{G} and C_{G}.

Thanks to the embedded RF bypass route, the maximum receiving power can be significantly enhanced. The linearity of the front-end circuit can also be relaxed while maintaining a good impedance matching condition. The implemented DPLL-based ADC with close-loop DAC feedback can further improve the RX dynamic-range without additional power and on/off-chip area. Finally, high sensitivity with a large input signal tolerant receiver can be realized within a minimized on-chip area.

3.4 High Efficiency and Harmonic-Suppressed Transmitter

A DFM TX shows potentially higher system efficiency compared with conventional Cartesian-TX while performing medium-rate FSK modulation [5, 96, 115–117]. Also benefits from its simple structure, the DFM is easier to be utilized in a compact BLE TX operating a 1-

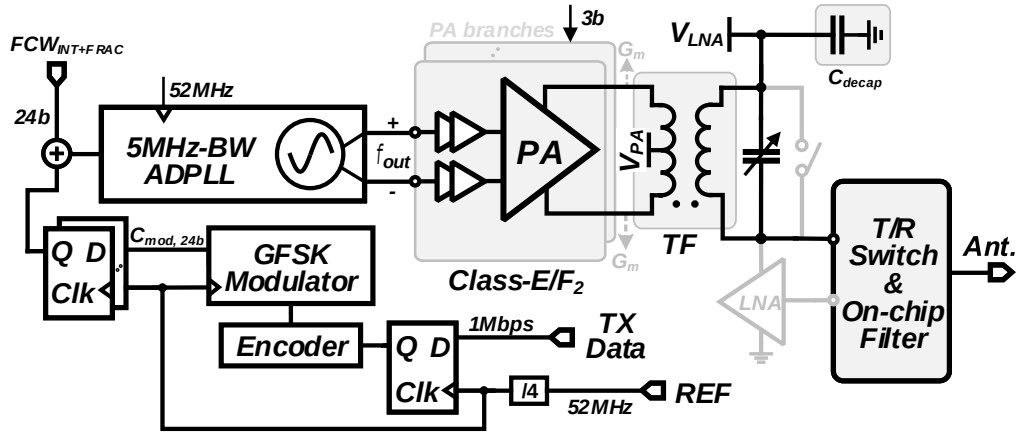


Figure 3.19: BLE transceiver in TX mode.

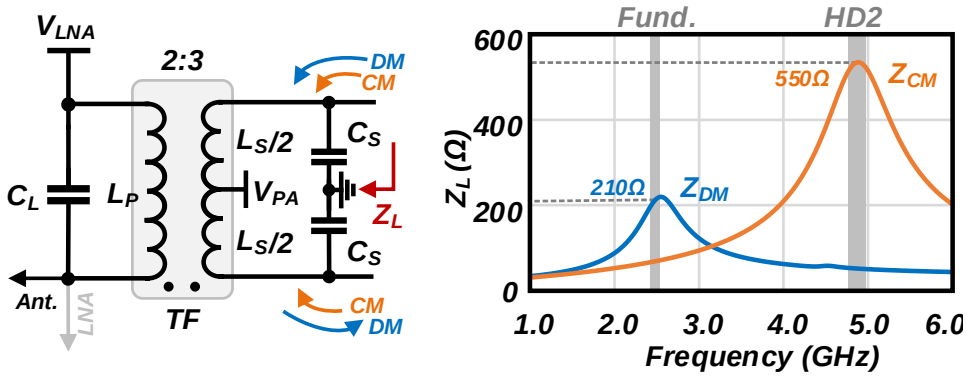


Figure 3.20: Transformer-based F_2 tank and simulated Z_L using DM/CM excitation.

Mbps GFSK modulation. The TX mode configuration of the BLE transceiver is shown in Fig. 3.19. The tested TX data is inputted from outside the chip and retimed with a 13-MHz clock. A 10-bit signed fixed-point number is generated from the encoder by using the retimed TX data. The GFSK filter with gain normalization generates a 24-bit number with a modulation index of 0.5 and a BT of 0.5. The FCW, which contains a 6-bit integer part and 18-bit fractional part, is added with the retimed modulator output C_{mod}. This number is fed into the DPLL with a gain of K_{DPLL} to generate the RF frequency, f_{out}, with 1-Mbps modulation information, which can be expressed as $f_{\text{out}} = (FCW + C_{\text{mod}}) \cdot K_{\text{DPLL}}$.

A low-power and 5 MHz-BW DPLL which benefits from the time-to-digital (TDC) range reduction [91] and the loop-latency reduction techniques [11] are implemented to achieve a low TX power consumption while realizing a sufficient TX modulation bandwidth.

3.4.1 HD2 Rejection

In this co-design of RFIO and PA, the inductor/transformer numbers are restricted to save chip area. As we notice that, a TF-based PA matching network can be exploited to impedance matching and harmonic suppression simultaneously, which benefits from its radically different characteristics between the differential-mode (DM) signal and the common-mode (CM) signal. A class-E/F_2 PA is implemented with a transformer-based matching network as shown in Fig. 3.19. To maximize the output power from a given device, specific load impedance (Z_L) should be presented at the device output [118]. Fig. 3.20 shows both of the simulated DM and CM impedances seen from the PA's drain node.

The transformer-based F_2 tank shown in Fig. 3.20 demonstrates two resonate frequencies ω_{CM} and ω_{DM}. Since the single-ended (SE) winding L_P and C_P are invisible for the CM signals because of the flux canceled by each other, the ratio ω_{CM}/ω_{DM} can be tuned simultaneously with adjusting the C_L which cooperating a fixed C_S. The resonate frequency at the CM excitation ω_{CM} is estimated as $1/\sqrt{L_S C_S/2}$, where C_S contains the parasitic capacitance from the PA and G_m as well as the transformer. Meanwhile, if the $0.5 \leq K_m \leq 1$, we have the $\omega_{DM} = 1/\sqrt{L_P C_{L,TX} + (L_S C_S)/2}$ according to [5]. To satisfy the ratio of the $\omega_{CM}/\omega_{DM} \approx 2$, the required $C_{L,TX}$ can be obtained via

$$\frac{C_{L,TX}}{C_S} \approx \frac{3L_S}{2L_P} = 3 \tag{3.11}$$

While analyzing the required $C_{L,RX}$ in RX mode, we have the DM resonate frequency $\omega_{DM,RX} \approx 1/\sqrt{L_P(C_{L,RX}+C_{LNA}) + (L_S C_S)/2}$. Thus, the relation between $C_{L,TX}$ and $C_{L,RX}$ can be evaluated as,

$$C_{L,TX} - C_{L,RX} \approx C_{LNA} \tag{3.12}$$

Therefore, capacitor C_L is designed to have 3 coarse bits to cover both TX/RX resonate mode, and 4 fine bits are also adopted for compensating the PVT variations. To assess the robustness of HD2 suppression, we carried out 200-run Monte Carlo simulations on process variations. The maximum value of HD2 is lower than -50 dBm at 0 dBm output power, as shown in Fig. 3.21.

3.4.2 HD3 Suppression

In order to achieve high-efficiency zero voltage switching (ZVS) operation, the inductive reactance L_S and L_P in the ISM band are optimized, respectively, while the capacitance C_{PA} and C_{LOAD} can be adjusted with SPI control codes. The tuning range of C_{LOAD}

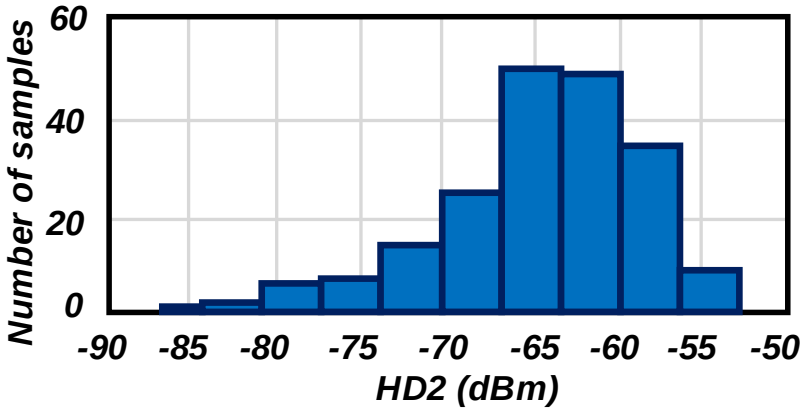


Figure 3.21: HD2 of TX output in 200-run Monte Carlo simulations with mismatch and process variations.

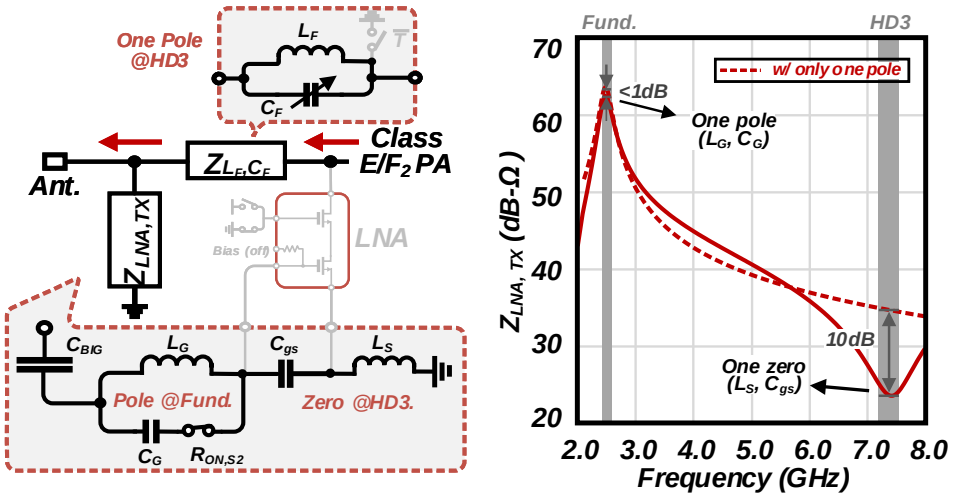


Figure 3.22: The proposed HD3 notch-filter reusing LNA input matching network.

is determined by incorporating the output capacitance of the transistor and the parasitic capacitance of the transformer. C_{LNA} also serves as a DC cut capacitor while the V_{LNA} with decoupling capacitors is implemented as the AC ground. With utilizing the tunable capacitor C_{LOAD} and C_{PA}, the TF-based differential PA can be configured into class-E/F_2 operation. The TX nominal output power is 0 dBm, which gives a voltage peak less than 1.4 V on transistor drain node with a 0.6 V supply voltage (V_{PA}).

As described in the Section 3.2, with a balanced transformer, the HD2 can be suppressed below -41 dBc. However, class-E PA generates significant HD3 component [119][120]. As we notice, there are two inductors that exist in the LNA matching network which can form an HD3 notch-filter based on LNA source degenerated inductor L_S while providing high enough impedance for fundamental frequency $f_{\mathrm{fund.}}$. Fig. 3.22 shows the proposed

HD3 notch-filter reusing LNA matching network, which has an impedance featuring a parallel resonance pole (L_G, C_G) and a series resonance (L_S, C_{gs}) zero. Compared with the conventional parallel resonant pole only structure [12], as the dashed line shown in Fig. 3.22, the proposed LNA input matching network, benefits from a reinforced HD3 suppression and approximately the same impedance at the desired frequency band.

To reuse the LNA matching inductors to construct a high-impedance for operation frequency with a notch characteristic for HD3 component, the appropriate values of L_G, C_G, L_S and C_{gs} have to be chosen such that the maximum of $Z_{LNA,TX}$ aligns with the operating frequency, which can be express as

$$Z_{LNA,TX} = \overbrace{(\frac{\omega L_G}{Q_G} + sL_G) \parallel (R_{ON,S2} + \frac{1}{sC_G})}^{Z_G,\text{Fund.}} + \frac{\omega L_S}{Q_S} + \underbrace{sL_S + \frac{1}{sC_T}}_{\text{HD3}} \tag{3.6}$$

The first item in the (3.6) represents the parallel impedance Z_G with considering the on-resistance $R_{ON,S2}$. The C_T represents the series capacitance from the C_{BIG}, C_{gs} and LNA transistor gate capacitance. In order to demonstrate the influence on TX efficiency from the on-resistance of $R_{ON,S2}$, the Z_G can be rewritten as:

$$Z_G = \frac{sL_G Z_{equiv.}}{Z_{equiv.} + sL_G + s^2 L_G C_G Z_{equiv.}} \tag{3.7}$$

In which,

$$Z_{equiv.} = \omega L_G Q_{L_G} \parallel R_{ON,S2} Q_{L_G}^2 \tag{3.8}$$

The insertion loss from a pair of resonator has been discussed in [80][8]. Note that for low-power LNA designs, a large gate inductance L_G (e.g., $> 10\,\text{nH}$) is typically implemented for low-power common source LNA input impedance matching due to the limited *gm* from relatively small transistor size [11, 93]. As indicated in the (3.8), the large inductance of L_G relaxes the transistor size of the shunt switch. The simulated characteristic of RX path with different $R_{ON,S2}$ are shown in Fig. 3.23. With a $140\,\mu m/60\,nm$ NMOS transistor with FBB technique [8] in a standard 65-nm process, which provides a $R_{ON,S2} \approx 4\,\Omega$, the insertion loss from the RX path can be reduced to 0.15 dB, thanks to a resonant impedance of more than 1 kΩ at the operating frequency realized with a relatively small switch transistor size. To minimize the HD3 component, the $sL_S + 1/sC_T$ should be chosen to create a zero at the location of HD3. A $1.3\,n$H L_S with small on-chip area ($Q_S \approx 10$) is adopted. Fig. 3.24 shows the simulated TX performances. 0.6 V DC sup-

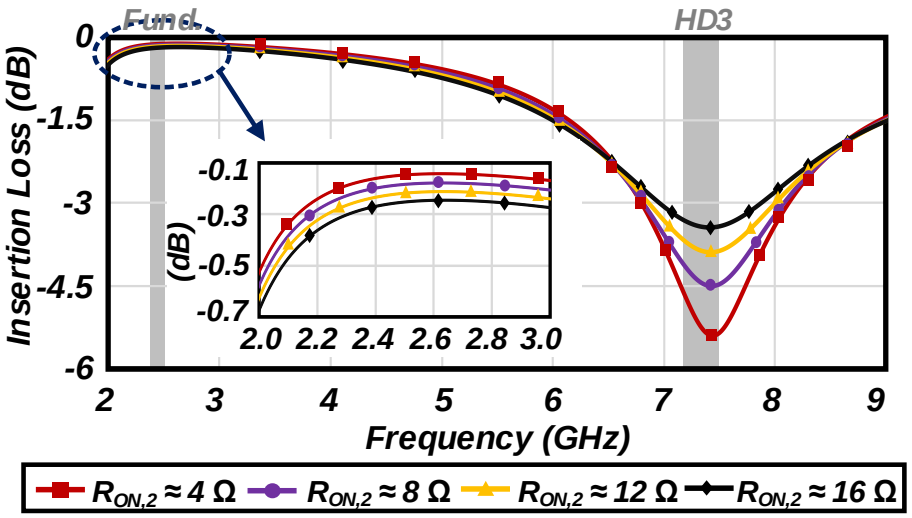


Figure 3.23: Insertion loss and low-pass characteristic of RX path in TX mode.

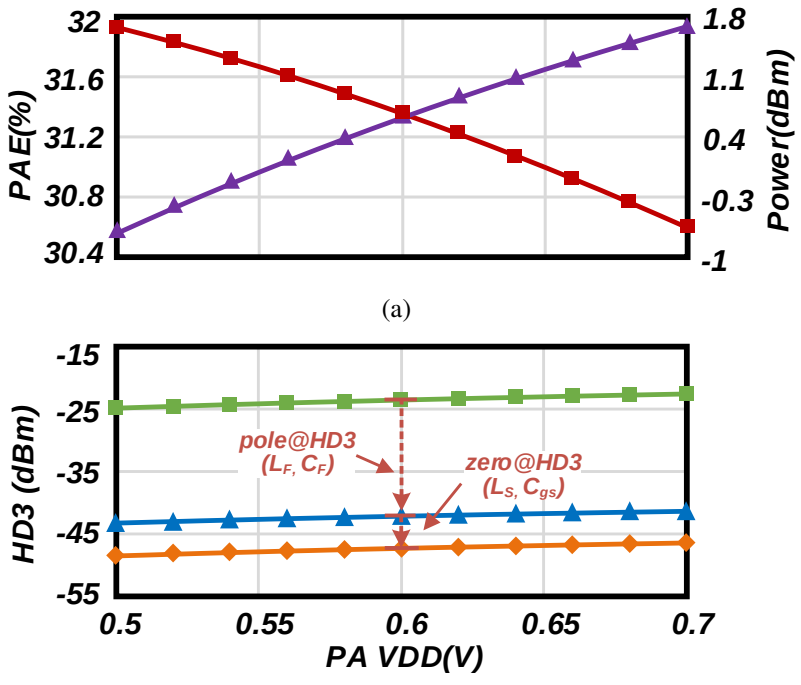


Figure 3.24: Simulated (a) PA efficiency and output power versus VDD and (b) HD3 with proposed TX matching network.

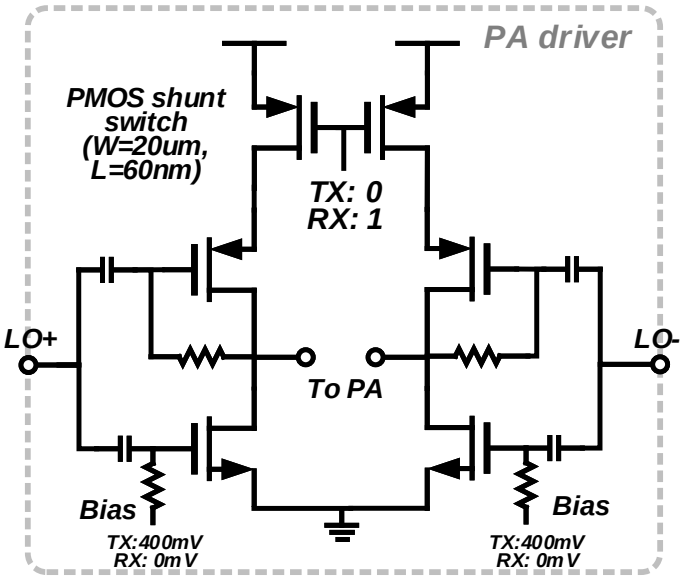


Figure 3.25: The driver of Class-D power amplifier.

ply is implemented in PA to generated 0 dBm power with 0.6 dB margin. In simulation, a 31.2 % power-added efficiency (PAE) is achieved with integrated filters and inverter-based drivers. Fig. 3.24(b) shows HD3 performances with the proposed TX matching network. The paralleling L_F and C_F provides 19 dB suppression. Meanwhile, by reusing the passive components in the LNA matching, the RX path also provides around 5.5 dB reinforced HD3 suppression from its bandpass/notch characteristic. Thanks to the wide bandwidth of the implemented DPLL, single-point direct frequency modulation can be realized. The low in-band phase noise and spur performances promise that the output signal spectrum meets the BLE requirements. Meanwhile, the low output power and far apart layout from the oscillator mitigate the pulling effect from the PA. The last stage of drivers are gated by using a large PMOS shunt transistor as shown in Fig. 3.25. In the simulation, the PA leakage is still around -45 dB (with PMOS shunt transistor is turned off, and the bias of driver is set to low). Considering the RX gain of the following stages (around 44 dB in minimum sensitivity case), this leakage will still have a big influence. With the shunt switch's help, this leakage can be reduced to lower than -80 dB, which can be negligible, as shown in Fig. 3.26.

The low-power DPLL, which only consumes 1 mW in TX mode, and a high-efficiency PA with harmonic-suppression network guarantees an 18.5% TX efficiency and fulfills the OOB harmonic emission requirements with fully on-chip integration.

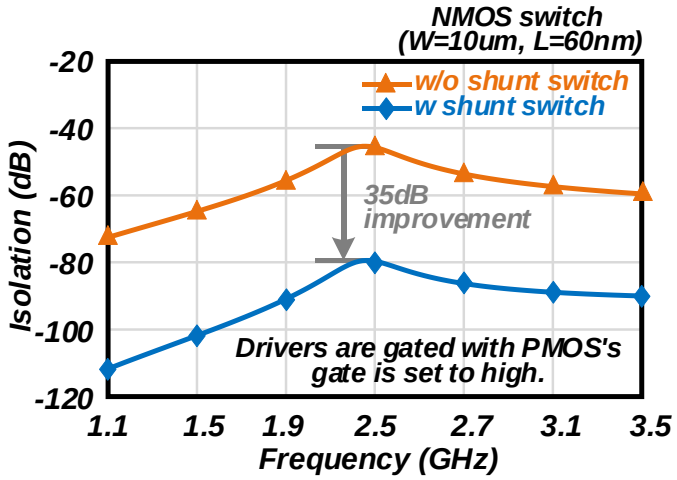


Figure 3.26: Simulated isolation of the PA driver with and without the shunt switch.

Table 3.3: START-UP TIME SUMMARY OF EACH COMPONENT IN BLE TRANSCEIVER

	Start-up Time
PLL	≤ 15 µs
Bias Generation	≤ 0.1 µs
RF Front-end	≤ 0.1 µs
TX/RX Switch	≤ 0.01 µs
Analog Baseband	≤ 1 µs
Total	< 17 µs

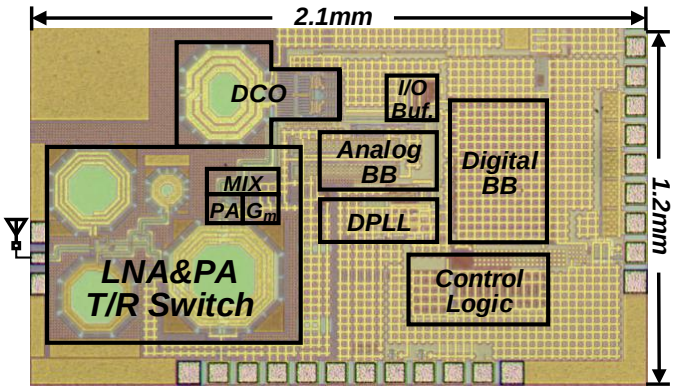


Figure 3.27: Chip micrograph of miniaturized BLE TRX.

Table 3.4: ON-CHIP AREA OF EACH PART

LNA&PA, T/R Switch	**0.56 mm^2**
Analog BB	**0.06 mm^2**
DPLL	**0.05 mm^2**
DCO	**0.18 mm^2**
Digital BB	**0.14 mm^2**
Control Logic	**0.12 mm^2**

3.5 Measurement Results

Note that all the BLE transceiver performances are measured with the constant carrier frequency (*e.g.,* 2.44 GHz), due to the lack of frequency hopping function in the presented BLE TRX design which only includes simply function of modulation and demodulation. Device identification, channel classification, channel information exchange, and adaptive frequency hopping these functions can only support by a complex digital baseband and has little relationship with the low-cost and low-power targets. In this design, only simply baseband with modulation and demodulation functions are embedded for the RX and TX measurements. However, for this design, the startup time is listed for each component in table 3.3. As specified in the BLE standard, the BLE transceiver hops at a rate of 1600 times per second over 40 2-MHz-wide channels. The time interval between two hops is around $1s/1600 = 625\mu s$. The longest startup time of the presented design is less than 17 µs. However, in the actual case, there are must be amounts of calibrations (*e.g.,* DC offset calibration and PA calibration and digital control logic (*e.g.,* MCU). The main startup time is still limited by these circuits.And based on startup time values, a fast frequency hopping can be realized, and the transceiver performances are not the bottom neck for the BLE frequency hopping speed. It is possible to include the frequency hopping function in the next BLE TRX design.

The T/R switch embedded BLE TRX is implemented in 65-nm CMOS technology. The chip micrograph is shown in Fig. 3.27. The on-chip area of each building blocks is shown in the following Table 3.4. This prototype of the miniaturized BLE TRX occupies only 0.85 mm^2 on-chip area, excluding the digital BB and control logic. Fig. 3.28 shows the exclusive RF port return loss in both TX and RX modes, obtained by using the Keysight N5247A. Across the Bluetooth Low Energy spectrum bandwidth of 83.5 MHz, the measured return loss is around -15 dB in both TX and RX high-gain operation modes. In the LNA bypass mode, the measured return loss also can achieve lower than -10 dB.

Fig. 3.29 plots the measured representative phase noise of the fractional-N DPLL and the phase noise with +10 dBm input power when the RX is on. The DPLL achieves an

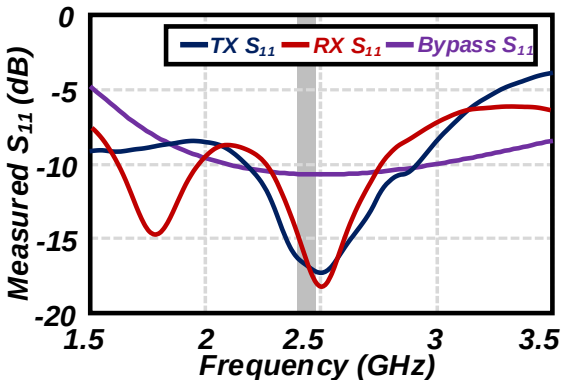


Figure 3.28: Measured return loss in TX and RX.

in-band phase noise of -110.7 dBc/Hz at 1-MHz offset frequency from 2.434 GHz. The measured in-band fractional spur of DPLL is -53 dBc. The close-loop DPLL shows an integrated PN of 0.76° (10 kHz∼20 MHz) with around 5-MHz bandwidth, which consumes 1 mW and 1.1 mW in TX and RX mode, respectively. A reference doubler has been integrated inside the DPLL, which provides 52 MHz doubled reference clock for the DPLL to achieve wide-bandwidth operation. The measured worst fractional spur is -51 dBc at around 6 kHz offset frequency. According to the blocker requirements (e.g.,± 3 MHz), a phase noise lower than -99 dBc/Hz is required while considering the most stringent ACR performance [11]. Common 26 MHz crystal, and input resistor feedback buffer can easily achieve -150 dBc/Hz at 3 MHz offset. The referred reference phase noise at 2.4 GHz is -110 dBc/Hz, which contributes less than TDC. For BLE application, -110 dBc/Hz is more than enough, and the in-band phase noise will still be dominated by TDC resolution, and reference noise contribution is negligible. A 26 MHz common crystal oscillator with PN lower than -150 dBc/Hz at 3MHz frequency offset, such as EPSON-TG2016 (-160 dBc@3MHz), can be potentially implemented and sufficient for BLE application.

The middle bump is not from the EM coupling and supply coupling. This disturbance is desired as the fundamental operation for this kind of receiver. Though the input FSK signal is down-converted and transported into the DCO. The DCO frequency changes according to the disturbance. However, if the ADPLL is active and the loop bandwidth is much wider than the maximum frequency of the disturbance, the ADPLL tries to keep the DCO frequency constant by adjusting the digital loop filter oppositely to disturbance [11]. As a result, the FSK signal can be extracted from the output of PLL's digital loop filter. Due to the DCO transfer function, there will be a bump show in the mid of the phase noise, which is desired baseband signal. The blue line is PLL and PA only, while PA's output is only -10 dBm. In the green line, PA is turned off, and the front-end is switched to bypass mode. Phase noise degradation may be caused by unexpected coupling from

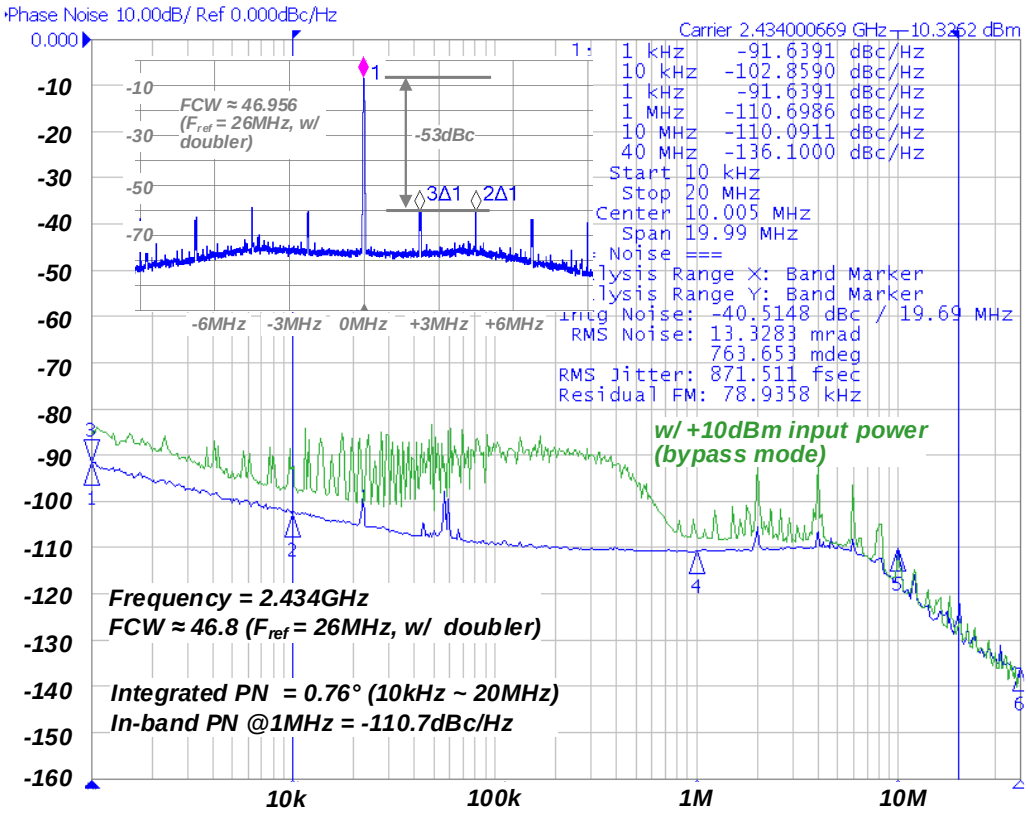


Figure 3.29: Measured DPLL phase noise and fractional spur with 26 MHz input reference clock (w/ reference doubler).

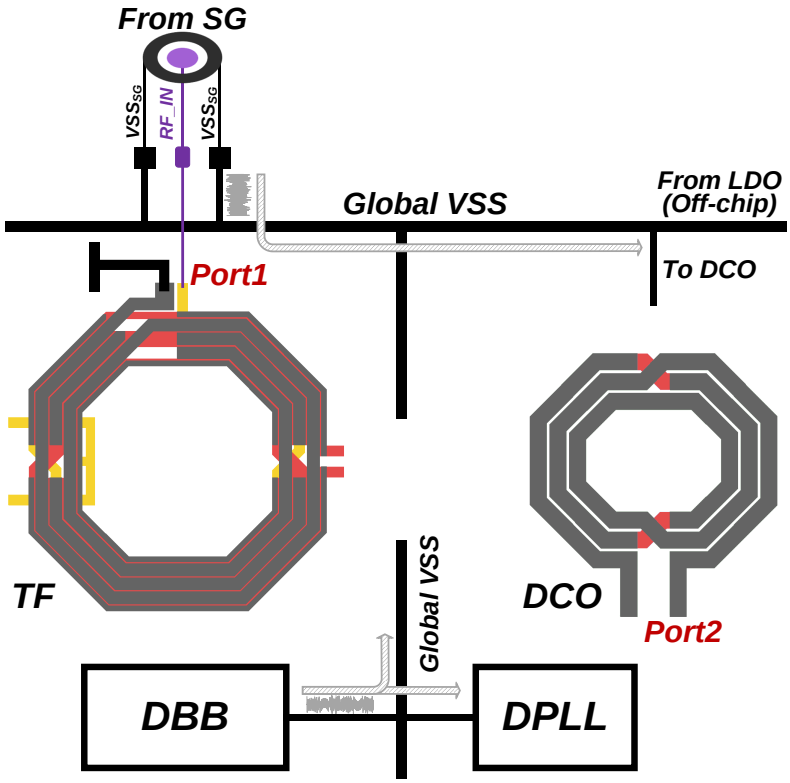
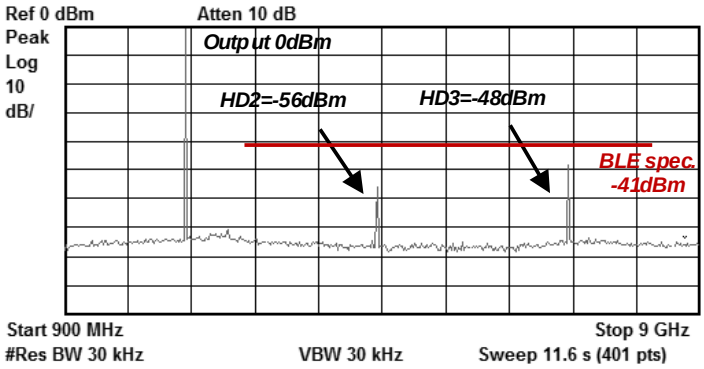


Figure 3.30: The noise source analysis of the degradation of the phase noise performance.

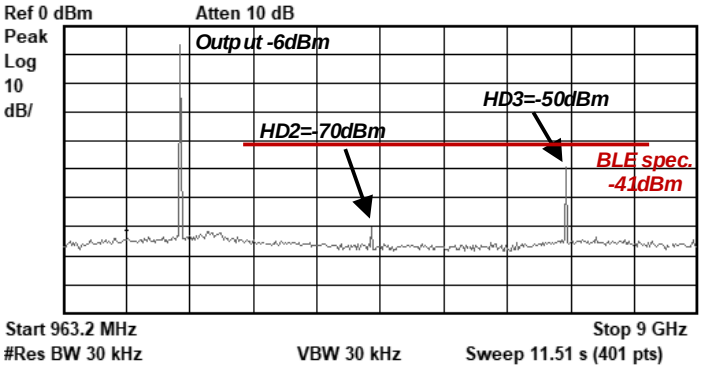
another test buffer (with resistor load), digital circuits, and equipment (SG). Due to the T/R switch implementation, the test buffer with high power consumption must be turned on to measure the PLL phase noise (PA is turned off). Since there is coupling from this buffer, PLL phase noise will be degraded. This degraded phase noise will not degrade NF performance and only slightly degrade interference rejection due to the 3MHz phase noise increment. In real RX operation, the test buffer is off, the disturbance from this buffer will disappear, and the phase noise may be better than the green line if Fig. 3.29. The measured flicker noise is degraded due to the narrow capture setting of the equipment (Keysight E5052B).

In addition, through the power supplies are separated, and in case of disturbance coupled from other circuits, there is only one global ground line for different parts of the circuit, as shown in Fig. 3.30. The external signal generator and digital baseband circuit pollute the global ground, which also influences some sensitivity circuits inside the DPLL, such as DCO, DTC, and TDC. Thus, a lot of noise spurious appears on the spectrum, which is coupled from the ground line.

Fig. 3.31 verifies the TX harmonic suppression performances through the conducted measurement at the middle-frequency channel (2.44 GHz). The suppression of TX-HD2



(a)



(b)

Figure 3.31: Measured TX typical harmonic: (a) 0 dBm output power; (b) -6 dBm output power.

Table 3.5: THE POWER COMPARISON OF EACH COMPONENT WITH STATE-OF-THE-ART BLE DESIGNS.

	This Work	[17]	[121]	[11]	[92]
LNA	0.7 mW (30%)	0.7 mW (28.5%)	0.69 mW (35.2%)	0.7 mW (30%)	1.36 mW (26.8%)
Gm		N.A.			
Mixer*	0	N.A.			
ABB	0.5 mW	0.8 mW	0.12 mW	0.5 mW	0.8 mW
ADC	0	0.25 mW	0	0	0
PLL(VCO)	1.1 mW	1.4 mW	1.15 mW	1.1 mW	2.92 mW

* mixer only, excluding LO buffer.

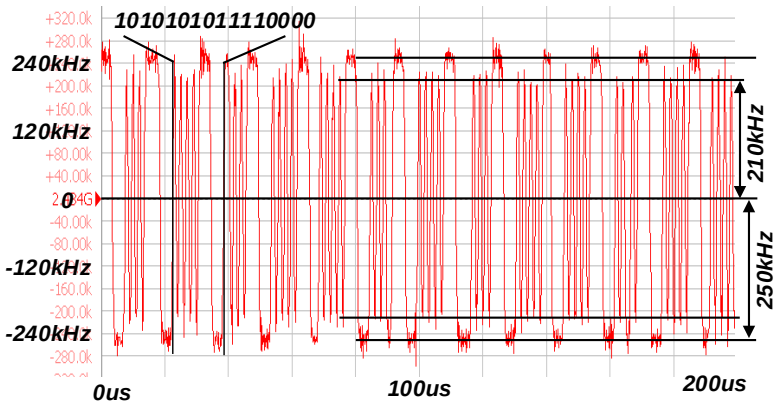
and TX-HD3 exceeds 56 dBc and 48 dBc, and it leaves 15 dB and 7 dB margin above the FCC spurious emission requirement (-41.2 dBm) respectively, while the TX delivers 0 dBm power to antenna with the four PA branches enabled, as shown in Fig. 3.31(a). In a -6 dBm output power condition, the TX-HD2 achieves -70 dBm harmonic level, and the TX-HD3 also achieves around the -50 dBm, which are plotted in Fig. 3.31(b). The harmonic performance of TX indicates the proposed miniaturized on-chip RFIO can avoid the dedicated on/off-chip filter for satisfying the harmonic requirements.

To measure the worst-case TX modulation deviation, a 10101011110000 data pattern is used. The measured maximum frequency drift is $\pm$40 kHz under this data pattern, as shown in Fig. 3.32(a). In Fig. 3.32(b) a 1.99% FSK error is achieved by using the digital modulation analysis function in a vector signal analyzer. The spectrum mask at 2.434 GHz using the maximum hold mode is shown in Fig. 3.32(c).

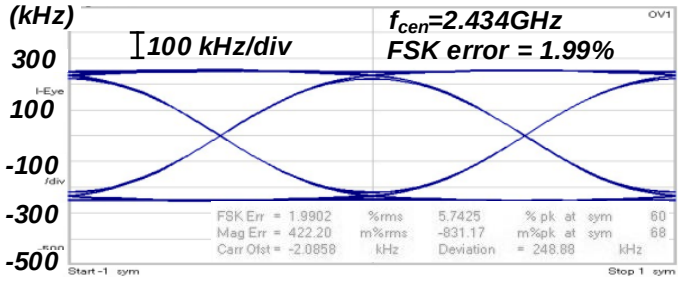
The interference performance of RX is measured with a -67 dBm wanted signal, as shown in Fig. 3.33. The ratio of the desired and interfering signal is plotted in Fig. 3.33(a) with bit error ratio (BER) just equal to 0.1%. The out-of-band (OOB) blocker performance is measured by using the same condition as the ACR measurement, which is shown in Fig. 3.33(b). Thanks to the good RX matching condition and the characteristic of the gain and linearity, the OOB blocker interference performance is satisfied with the BLE specification with sufficient margin.

The performances comparison of the T/R switch are summarized in Table 3.6. Even though almost the BLE transceiver implements a T/R switch, it is still difficult to find sufficient information about the switch design if the focus of the paper is not on the front-end design or T/R switch design. Meanwhile, it is difficult to extract the parameters of the T/R switch or LNA when the overall performances of BLE TRXs are reported.

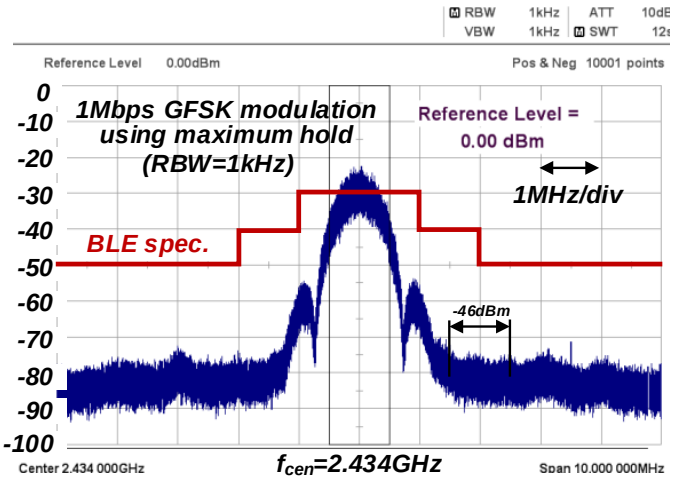
Fig. 3.34 shows the measured power breakdown of the TX and RX, including the digital baseband power. At the 0 dBm output power condition, the TX consumes 5.6 mW



(a)

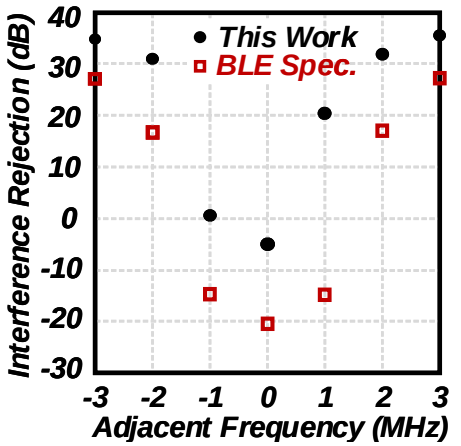


(b)

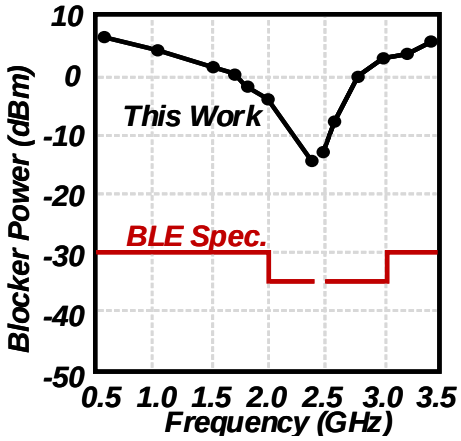


(c)

Figure 3.32: 1 Mbps GFSK output signal spectrum at 2.434GHz using maximum hold.

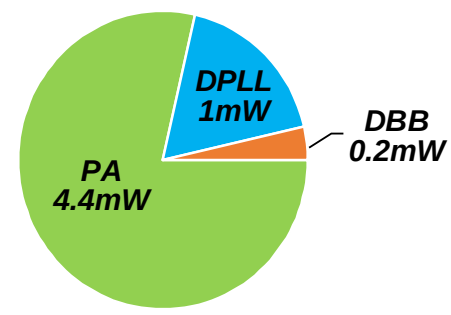


(a)

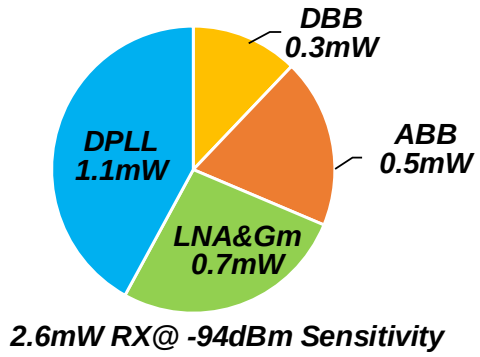


(b)

Figure 3.33: RX measurement results: (a) ACR with -67dBm signal input; (b) out-of-band blocker performance.



(a)



(b)

Figure 3.34: Breakdown of measured power: (a) TX mode with 0dBm output power (b) RX mode with minimum sensitivity.

Table 3.6: COMPARISON OF THE T/R SWITCHES.

	This Work	[7]	[8]	[9]	[17]
Tech.	65nm	90nm	180nm	350nm	28nm
LC Resonator Switch	Yes	Yes	Yes	No	Yes
LNA/PA Co-design	Yes	Yes	No	No	No
VDD	1	1.3	0.6/1.8	3.3	1.05
TX Insertion Loss	0.9*	<0.5	2.02/1.62	1.2	N.A.
Filter /LNA Bypass	Yes/Yes	No/No	No/No	No/No	Yes#/No
Return Loss (RX/TX, dB)	15/17	>10	>10	>15	>15
RX Isolation (dB)	>40*	16	17.15	>15	N.A.
LNA NF (dB)	3.84*	5.5	N.A.	N.A.	N.A.
P1dB (dBm)	>0	>30	>30	20.6	N.A.
Total Ind. Number	4	5	2	0	4
Area (mm^2)	0.56	N.A.	0.13**	N.A.	0.69**

* Simulated, ** Estimated, # HD2 only

Table 3.7: COMPARISON TABLE OF THE STATE-OF-THE-ART BLE TRANSCEIVERS

	This work		ISSCC'15 [12]	JSSC'17 [17]	ISSCC'17 [87]	JSSC'15 [86]	ISSCC'18 [88]	JSSC'18 [11]	ISSCC'15 [85]	TMTT'13 [84]
Technology	65nm		40nm	28nm	55nm	55nm	40nm	65nm	40nm	130nm
Modulation	GFSK (1Mbps)		GFSK (1Mbps)	GFSK (1Mbps)	GFSK (1Mbps)	GFSK (1Mbps)	GFSK (1Mbps)	GFSK (1Mbps)	GFSK (1Mbps)	GFSK (1Mbps)
Integration level	RF+DPLL+DBB		RF+PLL+PMU	RF+ADPLL	RF+PLL+DBB	RF+PLL+PMU	RF+DPLL+DBB	RF+DPLL+DBB	RF+PLL+DBB (SoC)	RF+PLL+ABB
Ant. Switch & On-chip Matching	Yes		Yes	Yes	Yes	Yes	No	No	No	Yes
RX Dynamic Range (dBm)	-94∼+10		-94.5∼N.A.	-95∼N.A.	-96.8∼N.A.	-94.5∼N.A.	-95∼N.A.	-94∼-10	-94∼N.A.	-81.4∼-7.5
RX Sensitivity (dBm)	-94		-95.4	-95	-96.8	-94.5	-95	-94	-94	-81.4
PLL Int. Jitter (ps)	0.87 (10kHz∼10MHz)		N.A.	0.98 (10kHz∼10MHz)	N.A.	N.A.	N.A.	0.87 (10kHz∼10MHz)	1.71 (1kHz∼100MHz)	N.A.
Integrated TX-HD Suppression	Yes		Yes	Yes	Yes	Yes	N.A.	N.A.	N.A.	N.A.
Output Power (dBm)	-6	0	0	0	+8	0	1.8	0	-2	1.6
TX HD2/HD3 (dBc)	-64/-50	-56/-48	-52/N.A.	-51/-48	-58/-64	-55/-54	-57.8/-65.8	N.A.	N.A.	-44.7/-33.4
TX Efficiency	9.7%	18.5%	13%	21%	7.9%	10%	25%	20%	15%	24.5%
TX Power (mW)	2.6	5.4	7.7	4.7	79.6	10.1	6.1	5	4.2	5.9
RX Power (mW)	2.3		6.3	2.75	12	11.2	2.3	2.3	3.3	1.1
On-Chip Inductors*	4		5	4	4	5	2	4	2	1
TRX Active Area (mm^2)	0.85		1.1	1.9	2.0	2.9	0.8	1.64	1.3	0.8

* except for LC-oscillator

Table 3.8: OFF-CHIP COMPONENTS COST REDUCTION

Name	Price (USD)	Type	Conventional	Proposal
Capacitor	0.006	Murata, GMR-series, 0.1μF	9	5
Inductor	0.015	Murata, LQW-series	4	0
XTAL-32kHz	0.16	Epson, FC-135	1	1
XTAL-32MHz	0.11	Murata, XRC-series	1	1
CC2541	1.39	TI, >1ku	1	1
PCB	0.014/mm^2	6 layer	0.084 20 mm x 30 mm	0.07 20 mm x 25 mm
Total Cost			**0.468**	**0.37**

power, which achieves 18.5% maximum TX efficiency. Thanks to the low-power circuit techniques and the hybrid structure implementation, RX consumes only 2.6 mW power at the maximum gain mode when -94 dBm sensitivity is measured through confirming the 0.1% BER performance. The implemented DPLL shows a good phase noise performance while maintaining a low power consumption. Table 3.7 summarizes the state-of-the-art BLE transceivers and the proposed BLE TRX. The proposed transceiver embedded with a T/R switch shows a lower power consumption with higher TX efficiency and large RX input power tolerant. Compared with the other BLE transceivers with fully integrated on-chip T/R switch, this work achieves the minimum TRX area without the need for external filters and matching networks.

3.6 Conclusion

A low-power BLE TRX embedded with T/R switch is demonstrated in 65-nm CMOS technology for IoT application. With the miniaturized on-chip RFIO, this transceiver compliant with BLE requirements with the fully on-chip integration. With reduced off-chip components number, the cost of total BLE modules can be reduced. The detailed cost of each off-chip components are listed in Table 3.8. For a conventional BLE SoC application (*e.g.,* CC2541), total 9 off-chip capacitors, 4 off-chip inductors, and two XTALs are required. By the way, the PCB cost is also reduced due to there are no inductors. The total calculated cost for each BLE SoC module is reduced by about 20%. Meanwhile, the die cost is also reduced due to the smaller on-chip size. However, it is hard to compare with commercial SoCs because of the lack of information(*e.g.,* chip area and process, package, and labor cost should also be considered.). Also, for the commercial products, SoC level design is required with much large on-chip required. Compared with other previous work [11], more than 30 % chip area is reduced, and the design achieves the reported smallest on-chip area with TX/RX switch function in state-of-the-art BLE transceiver designs.

In conclusion, the proposed BLE TRX will enable minimum size and long life-time IoT modules.

Chapter 4

Conclusion and Future Works

4.1 Conclusion of the Thesis

This research aimed to reduce the transceiver front-end chip area and power consumption, which includes the RF input and output circuits (*e.g.,* LNA, PA and matching network) and the frequency synthesizer. According to the author's knowledge, the central area occupation is from the RF front-end due to the passive components, which cannot be shrunk with the process scaling. There is four main proposed circuit design in this thesis.

The chapter 2 focus on the low-power and small area VCO design. As one of the center parts of the frequency synthesizer, the VCO takes a much larger area than other circuits. Meanwhile, to satisfy the transceiver's phase noise requirement, the oscillator type is limited to LC-type, and more than 200 µW power consumption is required in conventional LC-type VCO design. In this chapter, a new transformer-based VCO is presented with much lower power consumption and larger output amplitude (to reduce the power budget of the buffer). The performances of the VCO are derived from the analysis and verified in experiments. Based on this transformer-based VCO design, improvements are applied and integrated in two different applications. The first one is the area-reduced and supply pushing reduced VCO design. The PGS embedded TF used in this work indicates that the compact TRX layout can be realized with a smaller on-chip area. The proposed VCO's core area is only 0.12 mm^2, as same as the transformer itself. To mitigate the PN degradation from the voltage ripple introduced by the DC-DC converter in battery-powered portable devices, a supply pushing reduction loop is embedded with the VCO while consuming no additional voltage headroom and minimizing additional power. The second design based on the transformer-based VCO is the injection-locked multiplier. The low jitter clock synthesizer is one of the most demanding components in various systems. As we noticed, the commonly implemented type-II PLLs using low reference

frequency cannot provide sufficient voltage-controlled oscillator (VCO) noise suppression bandwidth, *e.g.,* < 1 MHz.

In contrast to PLLs, the injection-locked clock multipliers lock oscillation frequency to an integer multiplier number of reference clock by injection pulses, and the noise suppression bandwidth is much larger. Meanwhile, the power budget is relatively much smaller compared with traditional PLL designs. In this part, the flicker noise of the VCO is become significant due to the ILCM can only provide first-order in-band noise suppression. Thus, the transformer-based VCO's flicker noise is analyzed, and a high jitter performance clock multiplier is constructed. With a better understanding of the injection lock mechanism, the frequency modulation can also be applied by utilized the injection locking (the in-band spurious issue should be solved). With this ultra-low-power ILCM, the next transceiver design may save more power from the frequency synthesizer.

After discussing the VCO, a new transceiver RF input and output circuit are proposed with minimized on-chip area and providing a direct antenna interface. The key performances of power amplifier, low-noise amplifier, and T/R switch are difficult to be designed as the counterparts by using off-chip components due to the low-quality factor of on-chip inductors/transformers and non-ideal transistor characteristics. Obviously, the insertion loss of the T/R switch is significantly important since it results in the TX efficiency reduction and RX sensitivity reduction. It is possible to implement the conventional method such as the SPDT switch and PA with an additional filter network. However, these methods are not area efficient and power efficient. An integrated Radio-Frequency Input-Output (RFIO) embedded with transmitter/receiver (TX/RX) switch function and on-chip impedance matching is proposed. There are two RX routes shown in the proposed structure. One is with the LNA route, and another is the LNA bypass route. Moreover, the LNA bypass route shares the same route with TX output. In TX mode, TF realizes 2^{nd} harmonic rejection and power combining, while the LNA matching network provides HD3 suppression. In RX mode, different RX input routes can be configured according to the input strength. The TF enables a single-ended LNA solution and lower power consumption. Through maximally reusing the passive on-chip components, including but not limited to the inductors, a harmonic-suppressed TX and high input power tolerant RX can be realized within a small on-chip area with an embedded T/R switch function. Compared with other previous work [11], more than 30 % chip area is reduced, and the design achieves the reported smallest on-chip area with TX/RX switch function in state-of-the-art BLE transceiver designs.

4.2 Contribution of the Thesis

Firstly, a low-power VCO structure is proposed, which is suitable for IoT applications. The key point of designing a transformer-based VCO are illustrated and can be implemented in any low-power and moderate phase noise required VCO design case. The detailed analysis of the transformer-based oscillator is carried out and can be easily applied in other transformer-based circuits. The supply reduction technique is also suitable for low voltage supply oscillator design with DC-DC converters. On suitable occasions, the proposed ILCM can be very power efficient and provide extremely high jitter performances. Also, the frequency modulation is also realizable by utilizing the injection locking. Secondly, the proposed minimized on-chip RF input and output circuitry with embedded TX/RX switch is a candidate for a low-frequency transceiver with a small area required. The proposed technique can be applied in any low-frequency TDD transceivers with out-of-band spurious emission required. All the presented techniques in this thesis can be candidates for the next generation of BLE transceiver design. The transformer-based VCO can be utilized to reduce the power of the frequency synthesizer. The injection-locked multiplier can be utilized to further reduce the power consumption with modulation function. Similar RF input/output techniques can be applied in the next generation design because of almost the same RF requirements.

4.3 Bluetooth Transceiver Towards 5.2

In December 2019, the Bluetooth core specification was updated to version 5.2. The transmitter characteristics based on core specification V5.2 [4] and receiver characteristics are summarized in the Table 4.2 in chapter 1.3. Compared to the standard v4.2 and the newly released v5.2, the most important change in the transmitter is the 2 Mbps mode is introduced as an alternative option which uses the GFSK modulation with 500 kHz frequency derivation. The basic 1 Mbps mode is similar to the description in BLE v4.2. Also, to realize long-distance communication, which is important in the mesh network, a class I power option is also available in the BLE part of the newly released v5.2.

Firstly, in the future work, the integration of both the 1 Mbps and 2 Mbps GFSK modulation is the first target (also needs to be realized in a low-power implementation.). As we introduce in section 3.4, a direct frequency modulation (DFM) TX shows potentially higher system efficiency compared with conventional Cartesian-TX while performing medium-rate FSK modulation. Also, benefits from the wide bandwidth of the PLL (around 5 MHz), the direct frequency modulation transmitter can be realized with 1 Mbps (2 Mbps) GFSK modulation. By directly changing the frequency control word, the output

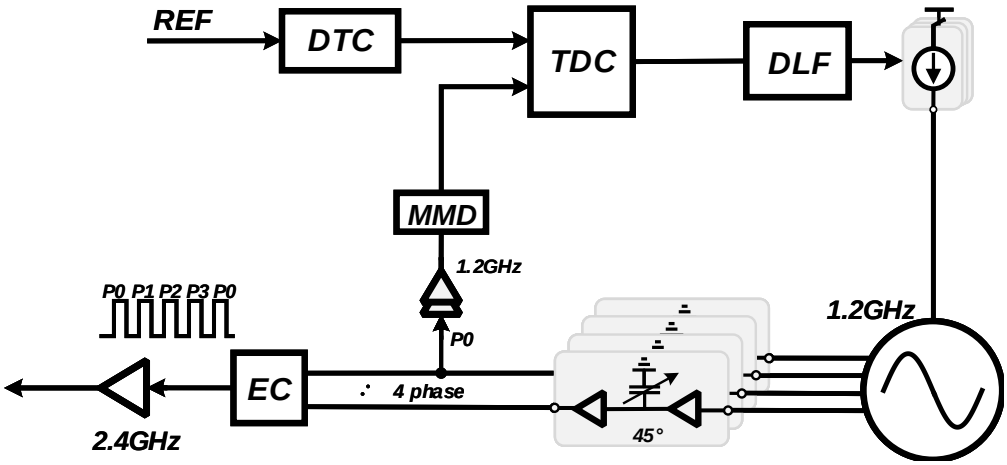


Figure 4.1: Simplified Transmitter Structure Based on CRRO.

of the DPLL can be modulated with 1 Mbps (2 Mbps) signal. In the TX part, there are also traditional ways to enhance the modulation bandwidth is that two-point modulation. Since the direct frequency modulation method is one point modulation at the frequency control word of the PLL, which experiences a low-pass loop function. While adding an additional modulation path at the input of the VCO, which has a high-pass loop function, a wider modulation bandwidth can be realized. However, several problems have been found in the traditional two-point modulation. Due to the different delay exists in the two modulation paths, the time and gain mismatch will occur and results in larger FSK error. Thus, additional delay mismatch and gain mismatch calibration circuits are required to realize two-point modulation, which needs additional power.

As we notice, the hybrid-loop RX can demodulate the signal (BW_{signal} ≈1 MHz) by utilizing its wide-bandwidth (BW_{PLL} ≈5 MHz). However, when the signal bandwidth increase, *e.g.,* 2 MHz, the input signal is filtered by the insufficient bandwidth of the PLL, which degrades the SNR and leads to a bad sensitivity performance.

There are several methods to overcome this problem. The first solution is that we can utilize a higher reference clock, *e.g.,* 80 MHz or higher, with a trade-off between the power consumption. However, this solution will double the power consumption of some building blocks in the DPLL, such as the DTC, TDC, and the digital filter. Also, conventional Cartesian-TRX can be utilized with I/Q demodulation, which needs more power consumed by the mixer, ADCs, and the circuit generating the I/Q signal. Since the hybrid-loop RX shows advantages in power consumption, to realize the 2 MHz signal demodulation, a bandwidth enhancement of the PLL has to be realized with an acceptable reference frequency.

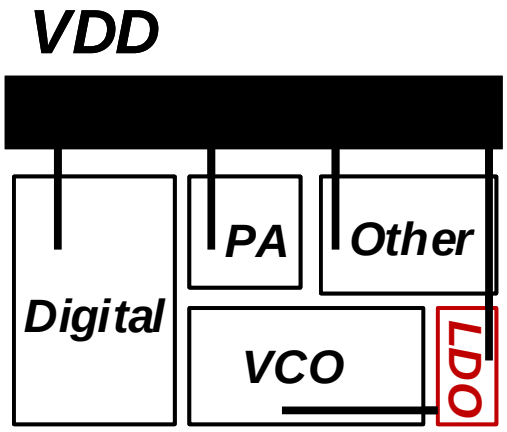


Figure 4.2: Power supply in conventional TX.

4.4 Small-Area and Low-Power TX using A Sub-200 μW Ring-Oscillator

In our future work, a low-power 2.4 GHz BLE direct frequency modulation transmitter is designed with a ring oscillator and 2 Mbps modulation is embedded using a low reference frequency *e.g.,* 40 MHz. Without using the higher reference frequency to enhance the PLL bandwidth or using the two-point modulation, a digital PLL based on a ring oscillator running at 1.2 GHz is utilized, as shown in Fig. 4.1. To generate the 2.4 GHz wanted frequency, an edge combiner can be utilized, which uses the multiple phases from the ring oscillator. With a 40 MHz reference bandwidth, the DPLL can be modulated with 250 kHz frequency derivation, and the EC combiner can double the frequency derivation into 500 kHz which satisfies the v5.2 requirements. Benefits from the EC combiner characteristic, the required frequency derivation can be reduced to only half of the original value.

A ring oscillator, which benefits from a wider tuning range with a small on-chip area can be utilized in this transceiver implementation. To realize a large frequency derivation, a large fine range tuning range is required for the PLL frequency control. The frequency tuning in the conventional ring oscillator can be realized by switching the loading capacitance as shown in Fig. 4.4 which wastes power. As we notice, the frequency is also related to the current consumption. Except adding the capacitor at each drain node, directly tuning the current can also the efficient in the frequency tuning, which saves more power (with a lower loading capacitance). Meanwhile, the frequency tuning of the ring oscillator can be realized by changing the number of branches, which consists of current mirror transistors and the switch transistors. Because the transistor is available in a wide

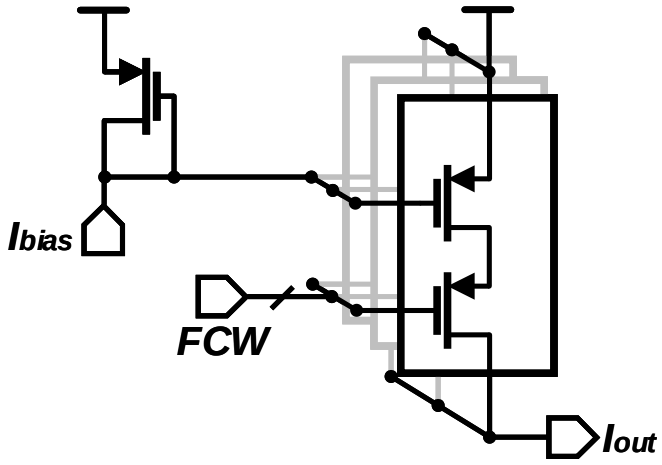


Figure 4.3: Current DAC implementation.

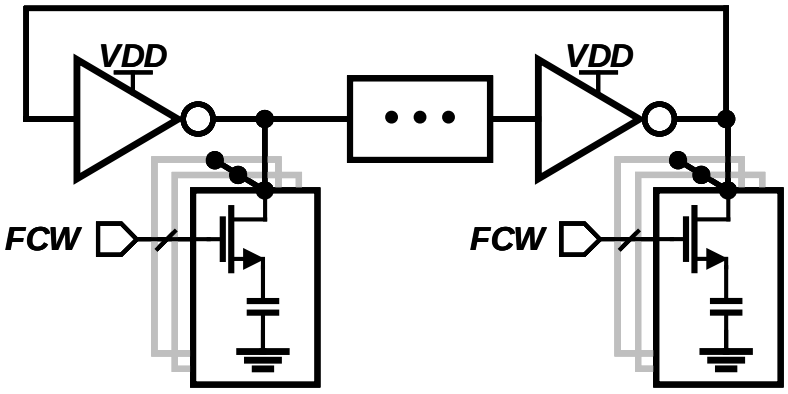


Figure 4.4: Conventional ring oscillator with frequency control bank.

range of sizes and can be matched in the layout, the current source implementation will be benefited from the smaller on-chip area (no capacitors) and the small mismatch between each cell. That improves the linearity of the fine frequency tuning with lower spur level is desired.

To lower the power consumption of the conventional ring oscillator design, a lower VDD, *e.g.,* 0.6 V, is commonly used, which needs additional LDO in the chip, which also consumes more power. As we also notice that the additional LDO has to be designed with large PSRR due to the large K_{VDD} of the ring oscillator, as shown in Fig 4.2.

The current source implementation can provide additional PSRR with an embedded frequency tuning function. The current source implementation and the current reused ring oscillator (CRRO) is shown in Fig. 4.5 while the inverter cell is shown in Fig. 4.6. By utilizing the characteristic of the edge combiner, the ring oscillator can run at 1.2 GHz, which saves nearly half of the power compared with the one running at 2.4 GHz. There are four cells in the ring oscillator design, and the stacked structure can be used to realize the

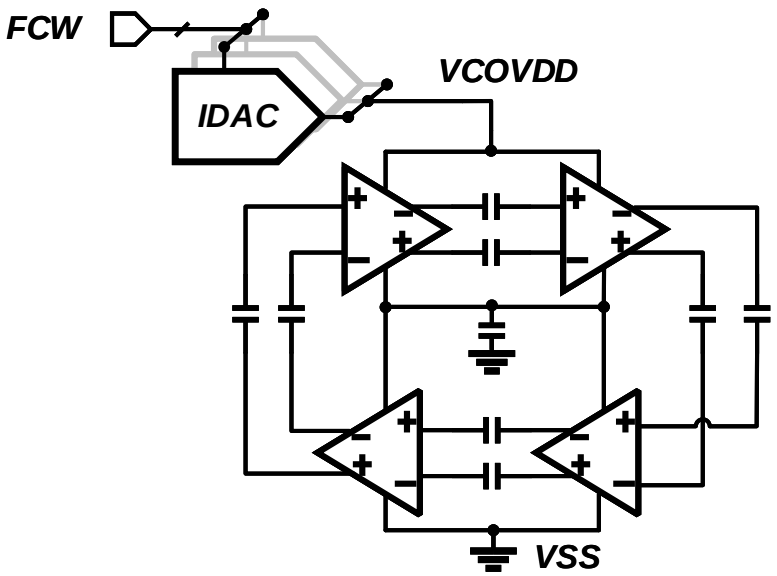


Figure 4.5: Proposed current reused ring oscillator with current DAC implementation.

current reuse-function. Since there are multiple phases in the ring oscillator, the virtual ground in the middle point can be easily realized with a 10 pF capacitor, and the voltage of the center point is approx to half of the VDD.

In this design, three current-steering DACs (3-bit coarse, 6-bit medium, 6-bit fine) are implemented to achieve frequency tuning range. A current bias is feed into a PMOS type current mirror, which generates the internal voltage bias for the current DAC. A transistor size ratio around 1:1 is chosen to mitigate the mismatch from the transistor, and thus, the internal current can precisely follow the feed current. The FCW control code is controlling the switch transistors to select the bleeding current. In case the parasitic capacitance influences the switching transition (more than 300 MHz frequency for the DSM control bit), the switch size has to be carefully selected with considering the on-state resistance and changing capacitance. Finally, only one finger 120n/200n transistor is selected as the fine band current switch and DSM switch. The target performance of the low-power ring oscillator and other state-of-the-art VCOs are summarized in Table 4.1.

4.5 BT 5.2 TRX with Multiple Power Mode

As we discussed in Section 1.3, transmitter characteristic has been a little bit changed *e.g.,* output power class, according to the core specification V5.2 [4] which summarized in the Table 4.2. Actually, the power enhancement of the transmitter brings great challenges to the local oscillator designs.

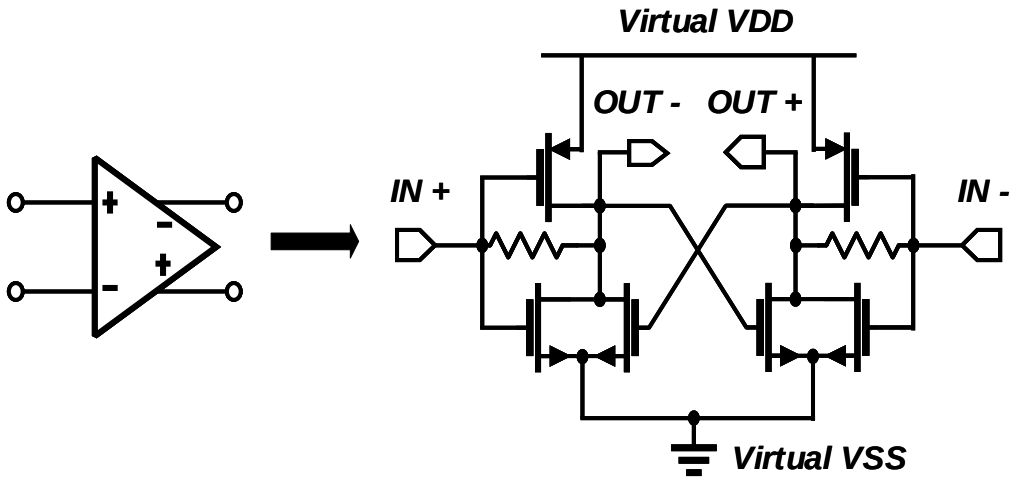


Figure 4.6: The inverter cell in current reused ring oscillator.

Table 4.1: COMPARISON WITH OTHER STATE-OF-THE-ART BLE VCOS

	JSSC'17	JSSC'19	JSSC'19	ESSCIRC'19	This Work (Target)
Technology	28nm	40nm	28nm	65nm	65nm
Structure	LC-VCO	Ring-Oscillator	LC-VCO	LC-VCO	Ring-Oscillator
Multi-Phase	No	Yes	No	No	Yes
Center Frequency (GHz)	2.454	2.25	2.4	2.68	1.275
PN@1MHz (dBc/Hz)	-116.9	-83∼-85	-119	-115.1	-88.5∼-91.2
Power (mW)	0.4	0.126	0.67	0.097	***0.12∼0.24***
Tuning Range (%)	22	22	N/A	N/A	45
FoM@1MHz(dBc/Hz')	-188.7	-158.1	-188.4	-194	-159∼-162.7
DCO Area(mm^2)	0.3	0.0017	0.15	0.28	0.0048
Supply Voltage (V)	0.5/1	0.6/0.9	0.2	0.5	***1***

Table 4.2: TRANSMITTER CHARACTERISTICS BASED ON CORE SPECIFICATION V5.2

Parameters		Value
Channels		f=2402+k*2 MHz, (k=0, ... ,39)
Output Power		Power Class 1:10dBm∼+20dBm Power Class 1.5: -20dBm∼+10dBm Power Class 2:-20dBm∼+4dBm Power Class 3: 0dBm∼-20dBm
Modulation Scheme		GFSK (0.5± 5% modulation index)
Frequency Deviation F_{min} = min { $\|F_{min+}\|$, F_{min-} }		1 Mbps: 250 KHz (F_{min}>185 KHz) 2 Mbps: 500 KHz (F_{min}>370 KHz)
Harmonic Emission	2nd harmonic	-41.2* dBm
	3rd harmonic	-41.2* dBm
In-band Spurious Emission	1 Mbps	2 MHz: -20 dBm
		≥ 3 MHz: -30 dBm
	2 Mbps	4,5 MHz: -20 dBm
		≥ 6 MHz: -30 dBm
Frequency Drift	Package	± 50 kHz (Maximum drift)
	Drift Rate	400 Hz/μS

* According to FCC 15.249.

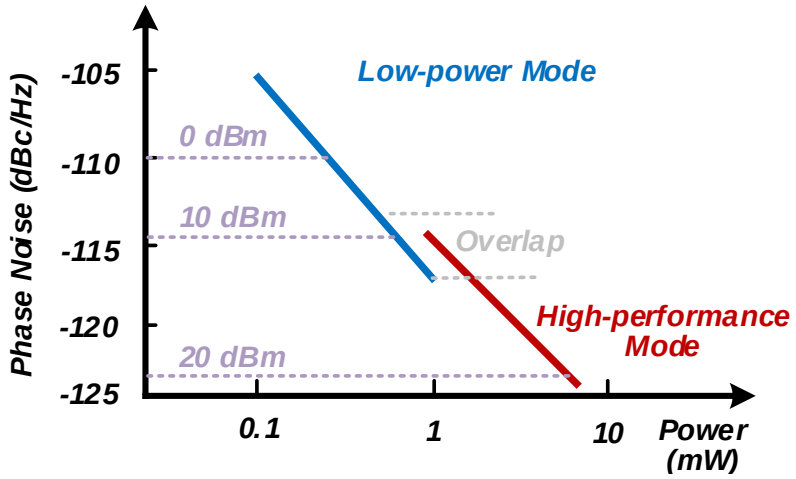


Figure 4.7: The phase noise coverage of the VCO with different modes.

First, we recollect the phase noise requirement for the RX and TX, respectively.

For the LO phase noise requirement in the RX, we mainly consider the ACR performance due to the reciprocal mixing because of the negligible SNR degradation introduced by the phase noise directly. When a large interference exists at the adjacent, the noise skirt of the VCO will down-convert the interference into the wanted signal in-band. Thus, the in-band SNR performance is degraded with a bad phase noise performance. Because of this, the PLL PN performances and the spur performance have to be considered seriously. The minimum required PN in the RX based on the most critical ACR performance can be calculated as:

$$\mathcal{L}_{\mathrm{PN,max}} \approx S_{\mathrm{wanted}} - S_{\mathrm{unwanted}} - SNR_{\mathrm{min}} - 10\log BW_{\mathrm{eff,noise}} \tag{4.1}$$

While considering the desired signal level with -67 dBm under a -40 dBm blocker at 3-MHz offset, a LO noise performance of less than -99 dBc/Hz at 3-MHz offset (-90 dBc/Hz at 1-MHz offset) is strictly required. This requirement is quite relaxed for a conventional LC-VCO design. Considering non-ideal components also contribute to the noise, the target of the VCO performance is specified with -110 dBc/Hz at 1 MHz offset are sufficient for the most strict ACR performance. This value is hard for the ring oscillator design but still very easy to realize with a custom-designed LC-VCO (even with low power consumption).

Let us consider the VCO phase noise requirement in the TX part. As we know, the TX in-band spurious emission is generated from the non-linearity of the TX chain or the phase noise or spurious of the frequency generators (PLLs). Also, as the table shows, the in-band spurious emission is specified in absolute value (dBm), which is measured on a 1 MHz

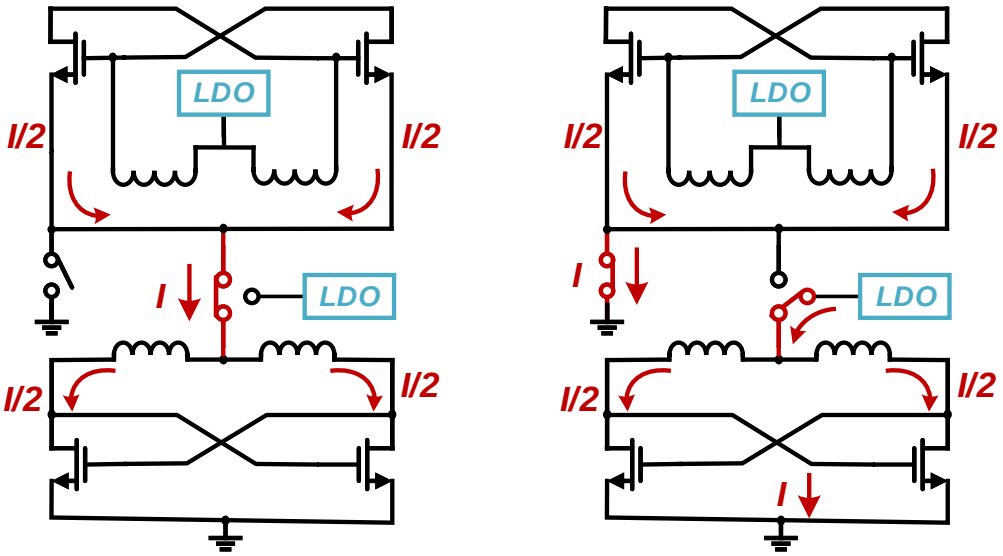


Figure 4.8: The mode switching in the transformer-based VCO structure.

RF frequency range. That means a higher output power requires a lower noise skirt of the PLL. Considering the 0 dBm cases, the PN noise with -110 dBm at 1 MHz offset leads to a enough margin (16 dB, shown in Fig 3.32(c)) in the 3 MHz ACR performance (the spur influence also needs to be considered). While considering the 10 dBm output cases, a PN noise with -124 dBc/Hz at 3 MHz offset is required which equals to -114 dBc/Hz at 1 MHz offset (10 dB margin). If a transmitter is embedded with power class I, the maximum output power of the TX will be around 20 dBm. That requires a more strict PN noise performance, which approx to -124 dBc/Hz at 1 MHz offset (10 dB margin). While considering the noise contribution from the spur and non-ideal components, this value should be enhanced accordingly. Basically speaking, the -124 dBc/Hz at 1 MHz offset phase noise performance is achievable in conventional LC-VCO design with several mWs power consumption. However, the integration of the low-power mode and the high-power mode is generally required. That means the VCO should have a large range of phase noise performances, which can be tuned by the mode selection, as shown in Fig. 4.7.

For example, a well-designed NMOS type LC-VCO can achieve -125 dBc/Hz at 1 MHz offset with 2 mW power consumption (FoM $\approx -190 dBc/Hz$). This performance is sufficient for the high power mode (>15 dBm) while this performance is much over in the low output cases (<0 dBm). Through changing the current bias of the NMOS-type VCO can achieve lower power consumption with decreased phase noise performances. However, the inductor value of the NMOS-type VCO already means that it is impossible to achieve low power consumption with a moderate phase noise performance. Another case is that the low-power design, which using large inductance. A CMOS-Type LC-VCO with a large inductor can be power-efficient in low-power cases with sufficient phase noise per-

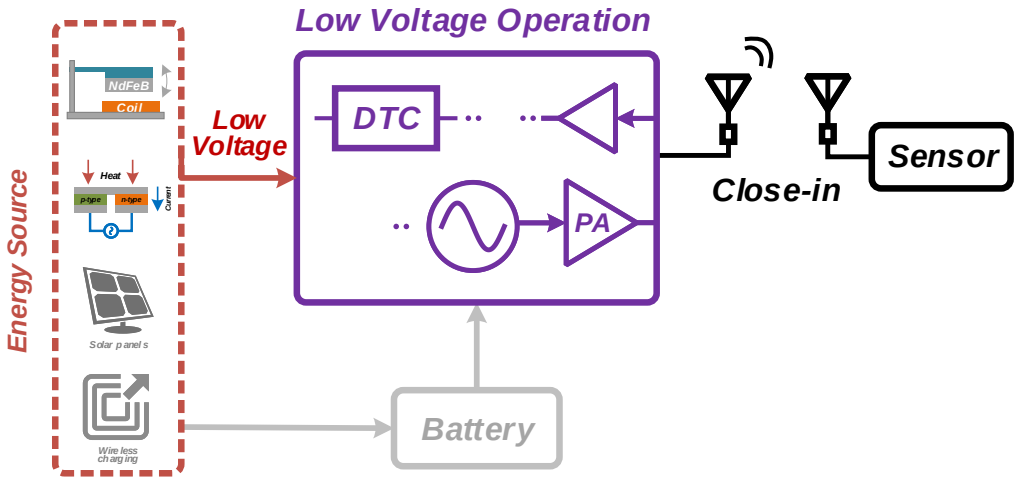


Figure 4.9: The low voltage operation of the BLE transceiver.

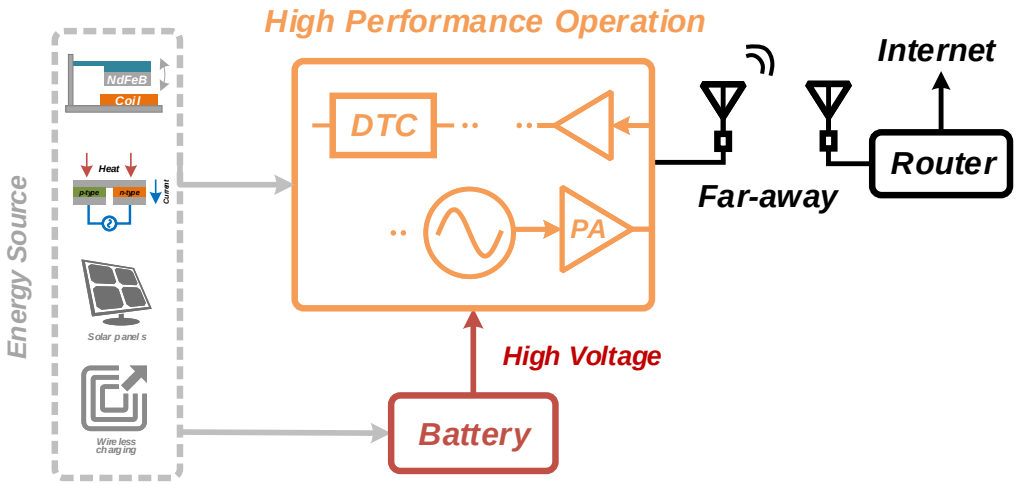


Figure 4.10: The high performance operation of the BLE transceiver.

formance. However, the phase noise performance is limited due to the inductance, and adding current does not significantly improve the effect, which will cause the transistor to work in the triode region.

Conventionally, to achieve both low power consumption in low output power case and high phase noise performance in high output case, two LC-VCO can be utilized, *e.g.,* one CMOS type and one NMOS type. However, this method requires a large on-chip area and design cost. Also, the LDO number needs to be double because the VDD condition is different in the NMOS-type and CMOS-type.

To save the on-chip area and realize a multi-mode of VCO design, the transformer-based structure can be utilized, which shown in Fig. 4.8. With properly configure the current path, the transformer can be configured into a current-reused mode, which is similar

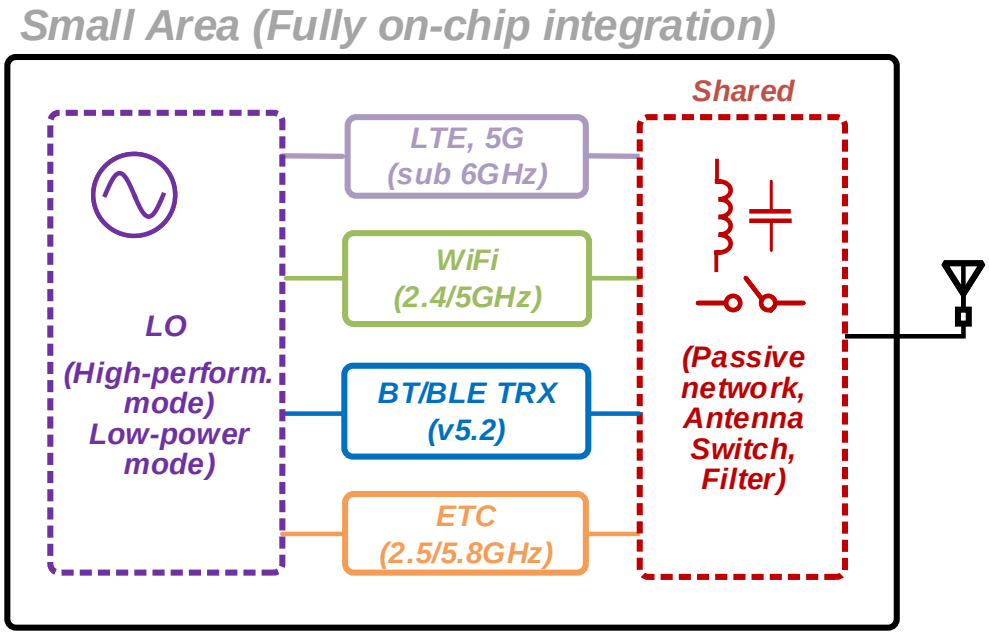


Figure 4.11: Multi-standard TRXs integration with low-cost implementation.

to the conventional CMOS structure. In the high-performance mode, the transformer-based structure can be configured into the coupled NMOS type. The total current will be double, while the voltage headroom will also be enhanced.

Also, the mode switching of other build blockers should also be considered, such as the DTC and TDC. Typically, a renewable energy source with lower voltage can be utilized in low-power mode, such as the solar panel with 0.5 v supply voltage as shown in Fig. 4.9. In this case, the DTC and the TDC should still work with moderate performance. However, the lower supply voltage will limit the current source in the DTC. Thus, some low-voltage techniques should be implemented in the low-power mode. While the high power mode can directly use the battery, which provides a higher voltage supply, as shown in Fig. 4.10, the power efficiency of these building blocks can be optimized.

Through mode switching in different scenarios, the power-efficiency of the TRX can be optimized while renewable energy sources can be implemented. Thus, the life-time of the transceivers can be greatly improved. And, we finally can achieve a better life at a lower cost.

As shown in Fig. 4.11, one passive filter with multi-pass bands can be implemented for the different standard TRXs. Such as the Bluetooth transceiver and the WiFi, which works in the same 2.4GHz. A shared passive network can be designed with different standard TRX. Also, the LO generation can be shared with the same band TRX operation. By sharing the area-consuming part, *e.g.,* the on-chip filter and the LO generation, also integrate the off-chip components, like the antenna switch, a small-area, and low-cost

multi-standard embedded TRX can be realized.

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Appendix A

Publication List

A.1 Journal Papers

- **Zheng Sun**, Hanli Liu, Dingxin Xu, Hongye Huang, Bangan Liu, Zheng Li, Jian Pang, Teruki Someya, Atsushi Shirane, and Kenichi Okada, "A Low-Jitter Injection-Locked Clock Multiplier Using 97 μW Transformer-Based VCO with 18-kHz Flicker Noise Corner," *IEICE Transactions on Electronics*, Vol.E104-C, No.7, Jul. 2021. (to be published)

- **Zheng Sun**, Hanli Liu, Hongye Huang, Dexian Tang, Dingxin Xu, Tohru Kaneko, Zheng Li, Jian Pang, Rui Wu, Wei Deng, Atsushi Shirane, and Kenichi Okada, "A 0.85 mm^2 BLE Transceiver Using an On-Chip Harmonic-Suppressed RFIO Circuitry with T/R Switch," *IEEE Transactions on Circuits and Systems I (TCAS-I)*, Vol. 68, No. 1, pp. 196-209, Jan. 2021, DOI: 10.1109/TCSI.2020.3033540.

- **Zheng Sun**, Dingxin Xu, Hongye Huang, Zheng Li, Hanli Liu, Bangan Liu, Jian Pang, Teruki Someya, Atsushi Shirane, and Kenichi Okada, "A Compact TF-based LC-VCO with Ultra-Low-Power Operation and Supply Pushing Reduction for IoT Applications," *IEICE Transactions on Electronics*, Vol.E103-C, No.10, Oct. 2020.

A.2 International Conferences

- **Zheng Sun**, Dingxin Xu, Junjun Qiu, Atsushi Shirane and Kenichi Okada, "A Small-area and High-efficiency BLE Transmitter with Duty-Cycled Edge-timing Calibration," *IEEE International Solid-State Circuits Conference*, Student Research Preview, 2021. (to be presented)

- **Zheng Sun**, Hanli Liu, Dingxin Xu, Hongye Huang, Bangan Liu, Zheng Li, Jian Pang, Teruki Someya, Atsushi Shirane, and Kenichi Okada "A 78fs RMS Jitter Injection-Locked Clock Multiplier Using Transformer-Based Ultra-Low-Power VCO," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Cracow, Poland, Sep. 2019.

- **Zheng Sun**, Hanli Liu, Dexian Tang, Hongye Huang, Tohru Kaneko, Rui Wu, Wei Deng, Kenichi Okada, "A 0.85mm^2 BLE Transceiver with Embedded T/R Switch, 2.6mW Fully-Passive Harmonic Suppressed Transmitter and 2.3mW Hybrid-Loop Receiver," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Dresden, Germany, Sep. 2018.

A.3 Domestic Conferences

- **Zheng Sun**, Dingxin Xu, Hongye Huang, 染谷 晃基, 白根 篤史, 岡田 健一, "A 78 fs RMS Jitter Injection-Locked Clock Multiplier Using Transformer-Based Ultra-Low-Power VCO", 電子情報通信学会 ソサイエティ大会 (於 大阪大学), C-12-22, Sep. 2019.

- **Zheng Sun**, Hanli Liu, Dexian Tang, Hongye Huang, 金子　徹, Rui Wu, Wei Deng, 染谷　晃基, 白根　篤史, 岡田　健一, "A T/R Switch Embedded BLE Transceiver with 2.6 mW Harmonic-Suppressed Transmitter and 2.3mW Hybrid-Loop Receiver", 電子情報通信学会 LSIとシステムのワークショップ (於 東京大学), May 2019.

- **Zheng Sun**, Hanli Liu, Dexian Tang, Hongye Huang, Tohru Kaneko, Rui Wu, Wei Deng, 染谷 晃基, 白根 篤史, 岡田 健一, "A 0.85 mm^2 BLE Transceiver with Embedded T/R Switch, 2.6 mW Harmonic Suppressed Transmitter and 2.3 mW Hybrid-Loop Receiver", 電子情報通信学会 集積回路研究会 (於 石垣島), March 2019.

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- **Zheng Sun**, Hanli Liu, Dexian Tang, Hongye Huang, 金子 徹, Wei Deng, Rui Wu, 白根 篤史, 岡田 健一, "An ADPLL-Centric Bluetooth Low-Energy Transceiver with 2.3 mW Interference-Tolerant Hybrid-Loop Receiver in 65-nm CMOS", 電子情報通信学会 LSIとシステムのワークショップ (於 東京大学), May 2018.

- **Zheng Sun**, Hanli Liu, Dexian Tang, Hongye Huang, 岡田 健一, 松澤 昭, "An ADPLL-Based High Interference Tolerant BLE Receiver with DAC Feedback Loop", 電子情報通信学会 総合大会 (於 東京電機大学), C-12-6, March 2018.

A.4 Co-Author

A.4.1 Journal Papers

- Jian Pang, Korkut Kaan Tokgoz, Shotaro Maki, Zheng Li, Xueting Luo, Ibrahim Abdo, Seitaro Kawai, Hanli Liu, **Zheng Sun**, Bangan Liu, Makihiko Katsuragi, Kento Kimura, Atsushi Shirane, Kenichi Okada, "A 28.16-Gb/s Area-Efficient 60-GHz CMOS Bidirectional Transceiver for IEEE 802.11ay," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 1, pp. 252-263, Jan. 2020.

- Bangan Liu, Yuncheng Zhang, Junjun Qiu, Hongye Huang, **Zheng Sun**, Dingxin Xu, Haosheng Zhang, Yun Wang, Jian Pang, Zheng Li, Xi Fu, Atsushi Shirane, Hitoshi Kurosu, Yoshinori Nakane, Shunichiro Masaki, and Kenichi Okada, "A Fully-Synthesizable Fractional-N Injection-Locked PLL for Digital Clocking with Triangle/Sawtooth Spread-Spectrum Modulation Capability in 5-nm CMOS," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 34-37, 2020.

- Hanli Liu, **Zheng Sun**, Hongye Huang, Wei Deng, Teerachot Siriburanon, Jian Pang, Yun Wang, Rui Wu, Teruki Someya, Atsushi Shirane, and Kenichi Okada, "A 265-μ W Fractional-*N* Digital PLL With Seamless Automatic Switching Sub-Sampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65-nm CMOS," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 54, no. 12, pp. 3478-3492, Dec. 2019.

- Hanli Liu, **Zheng Sun**, Dexian Tang, Hongye Huang, Tohru Kaneko, Zhijie Chen, Wei Deng, Rui Wu, and Kenichi Okada, "A DPLL-Centric Bluetooth Low-Energy Transceiver with a 2.3-mW Interference-Tolerant Hybrid-Loop Receiver in 65nm CMOS" *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 53, No. 12, Dec. 2018.

- Hanli Liu, Dexian Tang, **Zheng Sun**, Wei Deng, Huy Cu Ngo, and Kenichi Okada, "A Sub-mW Fractional-N ADPLL with FOM of -246 dB for IoT Applications," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 53, No. 12, Dec. 2018.

A.4.2 International Conferences

- Hanli Liu, **Zheng Sun**, Hongye Huang, Wei Deng, Teerachot Siriburanon, Jian Pang, Yun Wang, Rui Wu, Teruki Someya, Atsushi Shirane, Kenichi Okada, "A 265-μW Fractional-N Digital PLL with Seamless Automatic Switching Subsampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65nm

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- Jian Pang, Zheng Li, Ryo Kubozoe, Xueting Luo, Rui Wu, Yun Wang, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Takeshi Nakamura, Joshua Alvin, Daiki Matsumoto, Aravind Tharayil Narayanan, Bangan Liu, Junjun Qiu, Hanli Liu, **Zheng Sun**, Hongye Huang, Korkut Kaan Tokgoz, Keiichi Motoi, Naoki Oshima, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, Kenichi Okada. "A 28GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, Feb. 2019.

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A.4.3 Domestic Conferences and Workshops

- Dingxin Xu, **Zheng Sun**, Hongye Huang, 染谷 晃基, 白根 篤史, 岡田 健一, "A Time-Amplifier Gain Calibration Technique for ADPLL", 電子情報通信学会 ソサイエティ大会 (於 大阪大学), C-12-19, Sep. 2019.

- Hongye Huang, Hanli Liu, **Zheng Sun**, Dingxin Xu, 染谷 晃基, 白根 篤史, 岡田 健一, "A 2.4GHz Low-Power Subsampling/Sampling-Mixed Fractional-N All-Digital PLL", 電子情報通信学会 ソサイエティ大会 (於 大阪大学), C-12-18, Sep. 2019.

- Hongye Huang, Hanli Liu, **Zheng Sun**, 染谷 晃基, 白根 篤史, 岡田 健一, "A 0.85mm^2 BLE Transceiver with Embedded T/R Switch, 2.6mW Harmonic Suppressed Transmitter and 2.3mW Hybrid-Loop Receiver", 電子情報通信学会 集積回路研究会 (於 石垣島), March 2019.

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- Hongye Huang, **Zheng Sun**, Hanli Liu, Rui Wu, 染谷 晃基, 白根 篤史, 岡田 健一, "A 2.6mW BLE Transmitter Front-End with Fully-Passive Harmonic Suppression", 電子情報通信学会 ソサイエティ大会 (於 金沢大学), C-12-22, Sep. 2018.

- Hongye Huang, Hanli Liu, Dexian Tang, **Zheng Sun**, Wei Deng, Huy Cu Ngo, 白根 篤史, 岡田 健一, "An Ultra-Low-Power Fractional-N All-Digital PLL Using 10-bit Isolated Constant-Slope Digital-to-Time Converter", 電子情報通信学会 LSIとシステムのワークショップ (於 東京大学), May 2018.

- Hongye Huang, **Zheng Sun**, Hanli Liu, Dexian Tang, 岡田 健一, 松澤 昭, "Current-Reuse LNA for Low Power 2.4-GHz Receivers", 電子情報通信学会 総合大会 (於 東京電機大学), C-12-7, March 2018.

- Dexian Tang, Hanli Liu, **Zheng Sun**, Hongye Huang, 岡田 健一, 松澤 昭, "An Isolated Constant-Slope Digital-to-Time Converter", 電子情報通信学会 総合大会 (於 東京電機大学), C-12-33, March 2018.